HM5425161B Series
HM5425801B Series
HM5425401B Series

256M SSTL_2 interface DDR SDRAM
143 MHz/133 MHz/125 MHz/100 MHz
4-Mword × 16-bit × 4-bank/8-Mword × 8-bit × 4-bank/
16-Mword × 4-bit × 4-bank

HITACHI

ADE-203-1077 (Z)
Preliminary
Rev. 0.0
Jun. 28, 1999

Description

The HM5425161B, the HM5425801B and the HM5425401B are the Double Data Rate (DDR) SDRAM devices. Read and write operations are performed at the cross points of the CLK and the $\overline{CLK}$. This high speed data transfer is realized by the 2-bit prefetch piplined architecture. Data strobe (DQS) both for read and write are available for high speed and reliable data bus design. By setting extended mode resistor, the on-chip Delay Locked Loop (DLL) can be set enable or disable.

Features

- JEDEC standard compatible devices
- 2.5 V power supply
- SSTL-2 interface for all inputs and outputs
- Clock frequency: 143 MHz/133 Mhz/125 MHz/100 MHz
- Data inputs, outputs, and DM are synchronized with DQS
- 4 banks can operate simultaneously and independently
- Burst read/write operation
- Programmable burst length: 2/4/8
  - — Burst read stop capability
- Programmable burst sequence
  - — Sequential
  - — Interleave

Preliminary: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

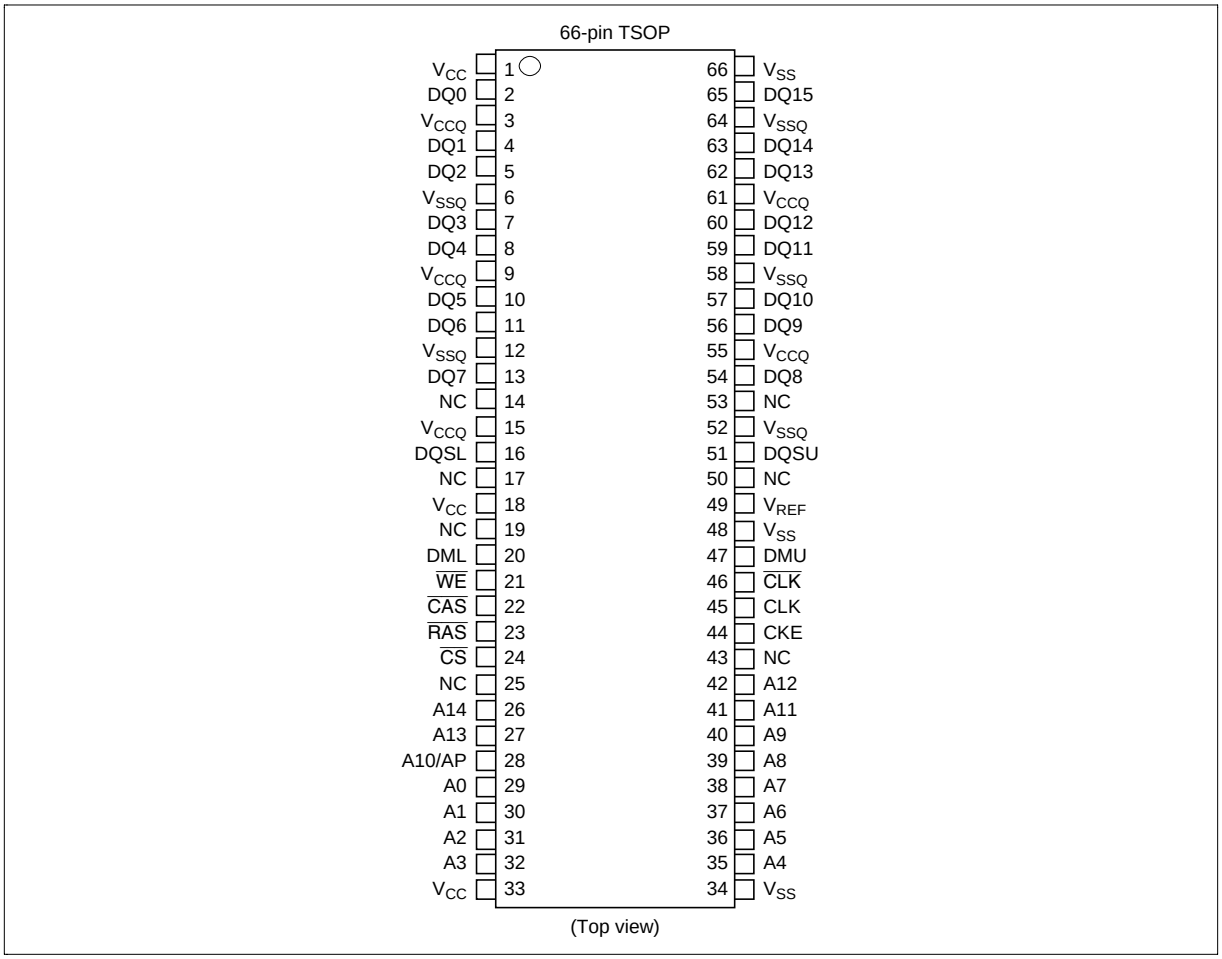
Hitachi semiconductor

- Start addressing capability
  - — Even and Odd
- Programmable $\overline{CAS}$ latency: 2/2.5
- 8192 refresh cycles: 7.8 μs (8192 row/64 ms)
- 2 variations of refresh
  - — Auto refresh
  - — Self refresh

Ordering Information

Type No.	Frequency	Package
HM5425161BTT-75A	143 MHz/133 MHz	400-mill 66-pin plastic TSOP II (TTP-66D)
HM5425161BTT-75B	133 MHz/100 MHz	
HM5425161BTT-10	125 MHz/100 MHz	
HM5425801BTT-75A	143 MHz/133 MHz	
HM5425801BTT-75B	133 MHz/100 MHz	
HM5425801BTT-10	125 MHz/100 MHz	
HM5425401BTT-75A	143 MHz/133 MHz	
HM5425401BTT-75B	133 MHz/100 MHz	
HM5425401BTT-10	125 MHz/100 MHz	

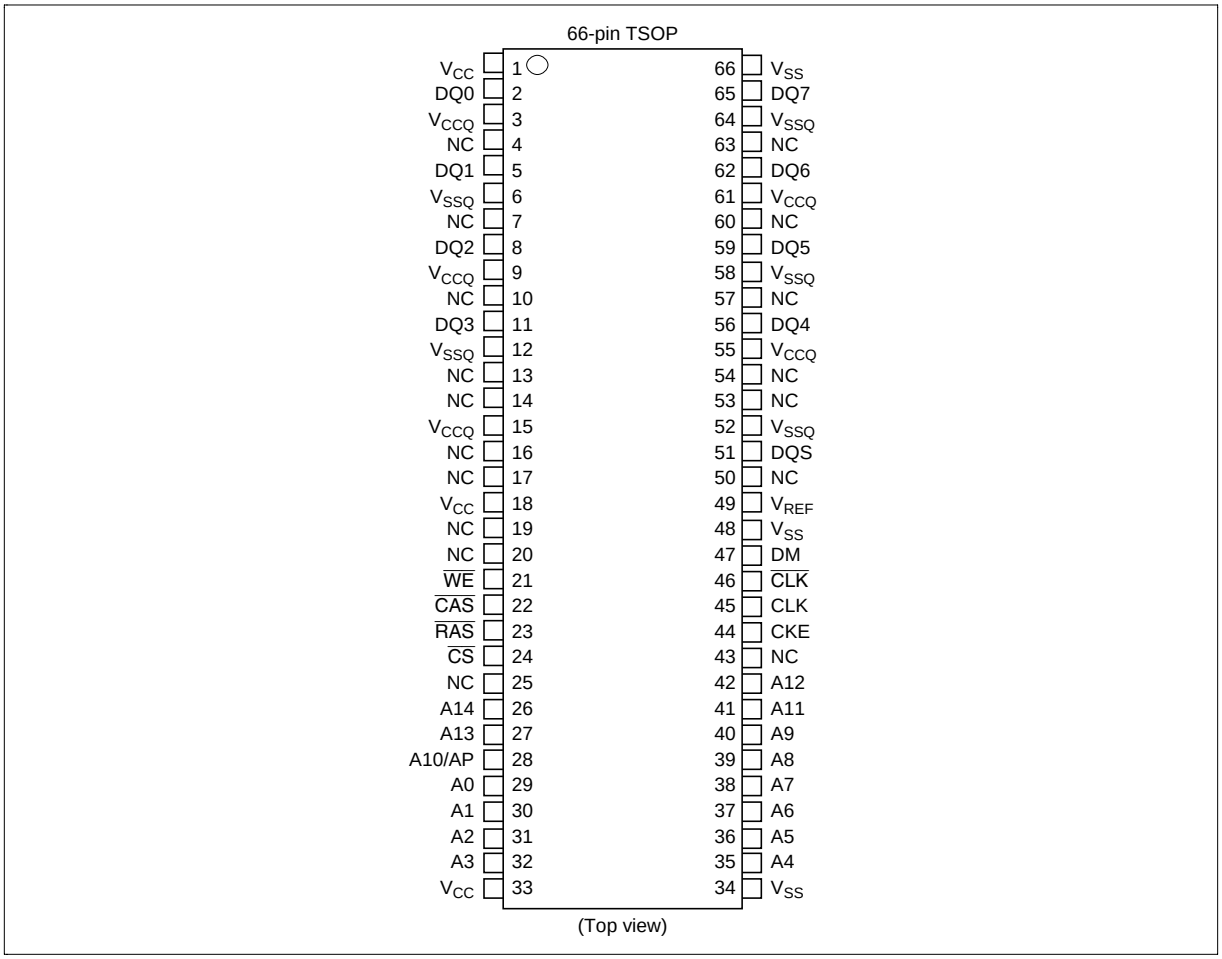
Pin Arrangement (HM5425161B)



Pin Description

Pin name	Function
A0 to A14	Address input — Row address A0 to A12 — Column address A0 to A8 — Bank select address A13 (BA1)/A14 (BA0)
DQ0 to DQ15	Data-input/output
DQSU	Upper input and output data strobe
DQSL	Lower input and output data strobe
$\overline{CS}$	Chip select
$\overline{RAS}$	Row address strobe command
$\overline{CAS}$	Column address strobe command
$\overline{WE}$	Write enable
DMU	Upper byte input mask
DML	Lower byte input mask
CLK	Clock input
$\overline{CLK}$	Differential clock input
CKE	Clock enable
V_{REF}	Input reference voltage
V_{CC}	Power for internal circuit
V_{SS}	Ground for internal circuit
V_{CCQ}	Power for DQ circuit
V_{SSQ}	Ground for DQ circuit
NC	No connection

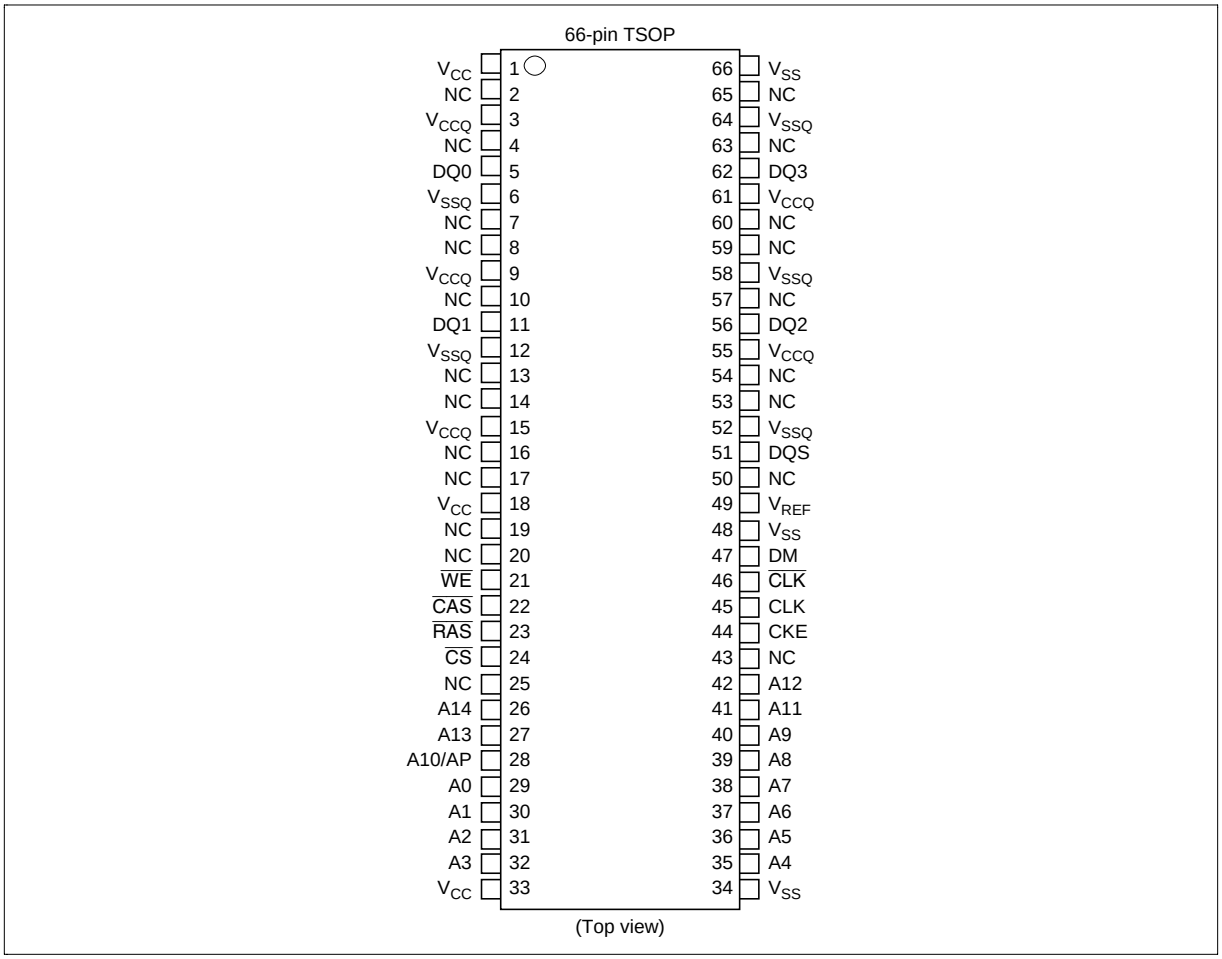
Pin Arrangement (HM5425801B)



Pin Description

Pin name	Function
A0 to A14	Address input — Row address A0 to A12 — Column address A0 to A9 — Bank select address A13 (BA1)/A14 (BA0)
DQ0 to DQ7	Data-input/output
DQS	Input and output data strobe
$\overline{CS}$	Chip select
$\overline{RAS}$	Row address strobe command
$\overline{CAS}$	Column address strobe command
$\overline{WE}$	Write enable
DM	Input mask
CLK	Clock input
$\overline{CLK}$	Differential clock input
CKE	Clock enable
V_{REF}	Input reference voltage
V_{CC}	Power for internal circuit
V_{SS}	Ground for internal circuit
V_{CCQ}	Power for DQ circuit
V_{SSQ}	Ground for DQ circuit
NC	No connection

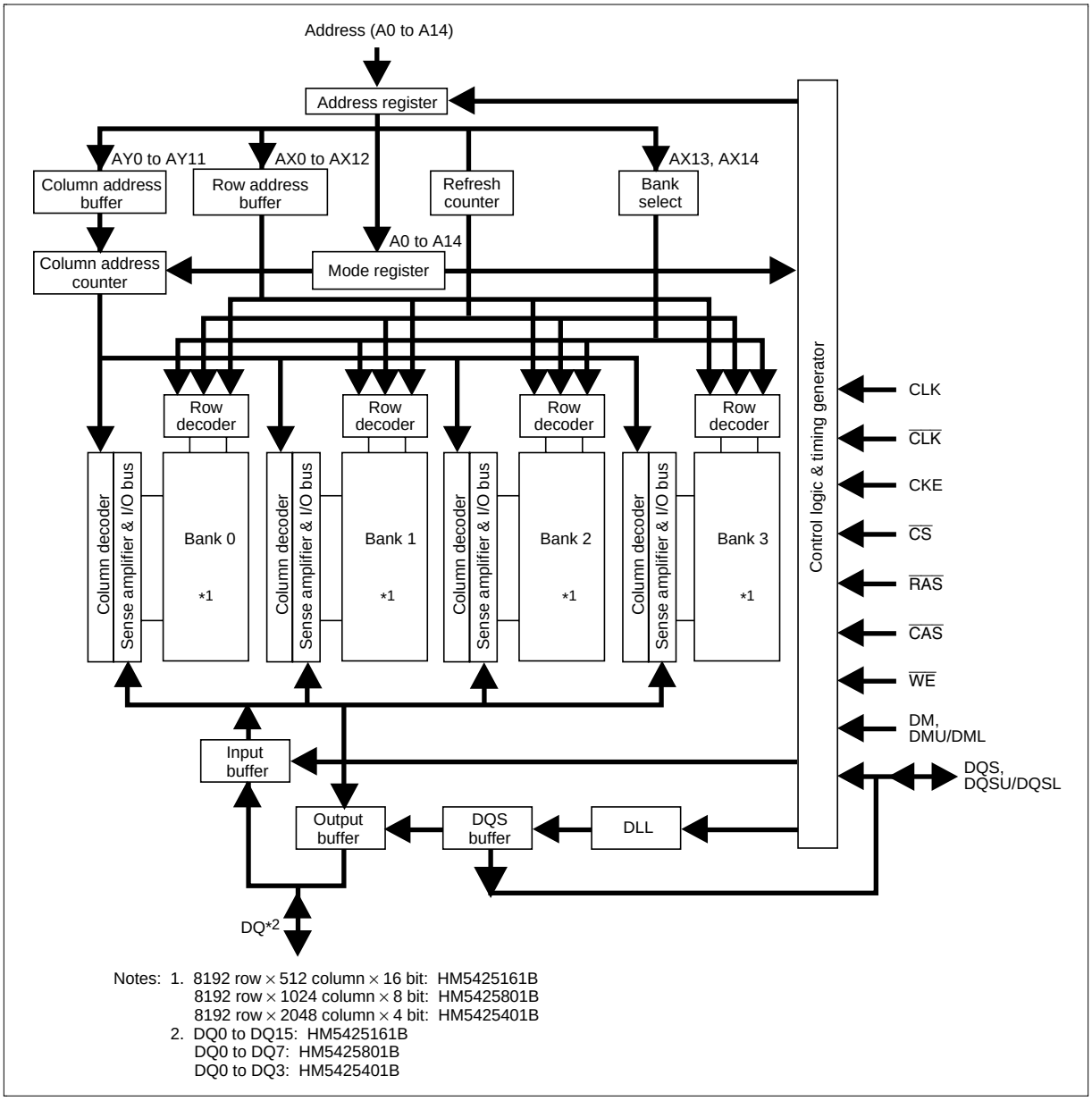
Pin Arrangement (HM5425401B)



Pin Description

Pin name	Function
A0 to A14	Address input — Row address A0 to A12 — Column address A0 to A9, A11 — Bank select address A13 (BA1)/A14 (BA0)
DQ0 to DQ3	Data-input/output
DQS	Output data strobe
$\overline{CS}$	Chip select
$\overline{RAS}$	Row address strobe command
$\overline{CAS}$	Column address strobe command
$\overline{WE}$	Write enable
DM	Input mask
CLK	Clock input
$\overline{CLK}$	Differential clock input
CKE	Clock enable
V_{REF}	Input reference voltage
V_{CC}	Power for internal circuit
V_{SS}	Ground for internal circuit
V_{CCQ}	Power for DQ circuit
V_{SSQ}	Ground for DQ circuit
NC	No connection

Block Diagram



Notes: 1. 8192 row × 512 column × 16 bit: HM5425161B
8192 row × 1024 column × 8 bit: HM5425801B
8192 row × 2048 column × 4 bit: HM5425401B
2. DQ0 to DQ15: HM5425161B
DQ0 to DQ7: HM5425801B
DQ0 to DQ3: HM5425401B

Pin Functions (1)

CLK, $\overline{\text{CLK}}$ (input pin): The CLK and the $\overline{\text{CLK}}$ are the master clock inputs. All inputs except DMs, DQSs and DQs are referred to the cross point of the CLK rising edge and the V_{REF} level. When a read operation, DQSs and DQs are referred to the cross point of the CLK and the $\overline{\text{CLK}}$. When a write operation, DMs and DQs are referred to the cross point of the DQS and the V_{REF} level. DQSs for write operation are referred to the cross point of the CLK and the $\overline{\text{CLK}}$.

$\overline{\text{CS}}$ (input pin): When $\overline{\text{CS}}$ is Low, commands and data can be input. When $\overline{\text{CS}}$ is High, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{WE}}$ (input pins): These pins define operating commands (read, write, etc.) depending on the combinations of their voltage levels. See "Command operation".

A0 to A12 (input pins): Row address (AX0 to AX12) is determined by the A0 to the A12 level at the cross point of the CLK rising edge and the V_{REF} level in a bank active command cycle. Column address (AY0 to AY8; the HM5425161B, AY0 to AY9; the HM5425801B, AY0 to AY9, AY11; the HM5425401B) is loaded via the A0 to the A9 at the cross point of the CLK rising edge and the V_{REF} level in a read or a write command cycle. This column address becomes the starting address of a burst operation.

A10 (AP) (input pin): A10 defines the precharge mode when a precharge command, a read command or a write command is issued. If A10 = High when a precharge command is issued, all banks are precharged. If A10 = Low when a precharge command is issued, only the bank that is selected by A13 (BA1)/A14 (BA0) is precharged. If A10 = High when read or write command, auto-precharge function is enabled. While A10 = Low, auto-precharge function is disabled.

A13 (BA1)/A14 (BA0) (input pin): A13 (BA1)/A14 (BA0) are bank select signals. The memory array is divided into bank 0, bank 1, bank 2 and bank 3. If A13 = Low and A14 = Low, bank 0 is selected. If A13 = High and A14 = Low, bank 1 is selected. If A13 = Low and A14 = High, bank 2 is selected. If A13 = High and A14 = High, bank 3 is selected.

CKE (input pin): CKE controls power down and self-refresh. The power down and the self-refresh commands are entered when the CKE is driven Low and exited when it resumes to High.

The CKE level must be kept for 1 CLK cycle (= t_{CKEPW}) at least, that is, if CKE changes at the cross point of the CLK rising edge and the V_{REF} level with proper setup time t_{IS}, by the next CLK rising edge CKE level must be kept with proper hold time t_{IH}.

Pin Functions (2)

DM, DMU/DML (input pins): DM (the HM5425801B and the HM5425401B), DMU/DML (the HM5425161B) are the reference signals of the data input mask function. DMs are sampled at the cross point of DQS and V_{REF}. DMU/DML provide the byte mask function. When DMU/DML = High, the data input at the same timing are masked while the internal burst counter will be count up. DML controls the lower byte (DQ0 to DQ7) and DMU controls the upper byte (DQ8 to DQ15) of write data.

DQ0 to DQ15 (input and output pins): Data are input to and output from these pins (the DQ0 to the DQ15; the HM5425161B, the DQ0 to the DQ7; the HM5425801B, the DQ0 to the DQ3; the HM5425401B).

DQS, DQSU/DQSL (input and output pin): DQS (the HM5425801B and the HM5425401B), DQSU/DQSL (the HM5425161B) provide the read data strobes (as output) and the write data strobes (as input). DQSL is the lower byte (DQ0 to DQ7) data strobe signal, DQSU is the upper byte (DQ8 to DQ15) data strobe signal.

V_{CC} and V_{CCQ} (power supply pins): 2.5 V is applied. (V_{CC} is for the internal circuit and V_{CCQ} is for the output buffer.)

V_{SS} and V_{SSQ} (power supply pins): Ground is connected. (V_{SS} is for the internal circuit and V_{SSQ} is for the output buffer.)

Command Operation

Command Truth Table

The HM5425161B, the HM5425801B and HM5425401B recognize the following commands specified by the $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and address pins. All other combinations than those in the table below are illegal.

		CKE									
Command	**Symbol**	**n – 1**	**n**	**$\overline{CS}$**	**$\overline{RAS}$**	**$\overline{CAS}$**	**$\overline{WE}$**	**BA1**	**BA0**	**AP**	**Address**
Ignore command	DESL	H	×	H	×	×	×	×	×	×	×
No operation	NOP	H	×	L	H	H	H	×	×	×	×
Burst stop in read command	BST	H	×	L	H	H	L	×	×	×	×
Column address and read command	READ	H	×	L	H	L	H	V	V	L	V
Read with auto-precharge	READA	H	×	L	H	L	H	V	V	H	V
Column address and write command	WRIT	H	×	L	H	L	L	V	V	L	V
Write with auto-precharge	WRITA	H	×	L	H	L	L	V	V	H	V
Row address strobe and bank active	ACTV	H	×	L	L	H	H	V	V	V	V
Precharge select bank	PRE	H	×	L	L	H	L	V	V	L	×
Precharge all bank	PALL	H	×	L	L	H	L	×	×	H	×
Refresh	REF	H	H	L	L	L	H	×	×	×	×
	SELF	H	L	L	L	L	H	×	×	×	×
Mode register set	MRS	H	×	L	L	L	L	L	L	L	V
	EMRS	H	×	L	L	L	L	L	H	L	V

Notes: 1. H: V_{IH}. L: V_{IL}. ×: V_{IH} or V_{IL}. V: Valid address input
2. The CKE level must be kept for 1 CLK cycle (= t_{CKEPW}) at least.

Ignore command [DESL]: When $\overline{CS}$ is High at the cross point of the CLK rising edge and the V_{REF} level, every input are neglected and internal status is held.

No operation [NOP]: As long as this command is input at the cross point of the CLK rising edge and the V_{REF} level, address and data input are neglected and internal status is held.

Burst stop in read operation [BST]: This command stops a burst read operation, which is not applicable for a burst write operation.

Column address strobe and read command [READ]: This command starts a read operation. The start address of the burst read is determined by the column address (AY0 to AY8; the HM5425161B, AY0 to AY9; the HM5425801B, AY0 to AY9, AY11; the HM5425401B) and the bank select address (BA). After the completion of the read operation, the output buffer becomes High-Z.

Read with auto-precharge [READA]: This command starts a read operation. After completion of the read operation, precharge is automatically executed.

Column address strobe and write command [WRIT]: This command starts a write operation. The start address of the burst write is determined by the column address (AY0 to AY8; the HM5425161B, AY0 to AY9; the HM5425801B, AY0 to AY9, AY11; the HM5425401B) and the bank select address (BA).

Write with auto-precharge [WRITA]: This command starts a write operation. After completion of the write operation, precharge is automatically executed.

Row address strobe and bank activate [ACTV]: This command activates the bank selected by A13/A14 (BA) and determines a row address (AX0 to AX12). When A13 = A14 = Low, bank 0 is activated. When A13 = High and A14 = Low, bank 1 is activated. When A13 = Low and A14 = High, bank 2 is activated. When A13 = A14 = High, bank 3 is activated.

Precharge selected bank [PRE]: This command starts a pre-charge operation for the bank selected by A13/A14.

Precharge all banks [PALL]: This command starts a precharge operation for all banks.

Refresh [REF/SELF]: This command starts a refresh operation. There are two types of refresh operation, one is auto-refresh, and another is self-refresh. For details, refer to the CKE truth table section.

Mode register set/Extended mode register set [MRS/EMRS]: The DDR SDRAM has the two mode registers, the mode register and the extended mode register, to defines how it works. The both mode registers are set through the address pins (the A0 to the A14) in the mode register set cycle. For details, refer to "Mode register and extended mode register set".

CKE Truth Table

		CKE							
Current state	**Command**	**n – 1**	**n**	**$\overline{CS}$**	**$\overline{RAS}$**	**$\overline{CAS}$**	**$\overline{WE}$**	**Address**	**Notes**
Idle	Auto-refresh command (REF)	H	H	L	L	L	H	×	2
Idle	Self-refresh entry (SELF)	H	L	L	L	L	H	×	2
Idle	Power down entry (PDEN)	H	L	L	H	H	H	×	
		H	L	H	×	×	×	×	
Self refresh	Self refresh exit (SELFX)	L	H	L	H	H	H	×	
		L	H	H	×	×	×	×	
Power down	Power down exit (PDEX)	L	H	L	H	H	H	×	
		L	H	H	×	×	×	×	

Notes: 1. H: V_{IH}. L: V_{IL}. ×: V_{IH} or V_{IL}.
2. All the banks must be in IDLE before executing this command.
3. The CKE level must be kept for 1 CLK cycle (= t_{CKEPW}) at least.

Auto-refresh command [REF]: This command executes auto-refresh. The banks and the ROW addresses to be refreshed are internally determined by the internal refresh contoroller. The average refresh cycle is 7.8 µs. The output buffer becomes High-Z after auto-refresh start. Precharge has been completed automatically after the auto-refresh. The ACTV or MRS command can be issued t_{RFC} after the last auto-refresh command.

Self-refresh entry [SELF]: This command starts self-refresh. The self-refresh operation continues as long as CKE is held Low. During the self-refresh operation, all ROW addresses are repeated refreshing by the internal refresh contoroller. A self-refresh is terminated by a self-refresh exit command.

Power down mode entry [PDEN]: t_{PDEN} (= 1 cycle) after the cycle when [PDEN] is issued. The DDR SDRAM enters into power-down mode. In power down mode, power consumption is suppressed by deactivating the input initial circuit. Power down mode continues while CKE is held Low. No internal refresh operation occurs during the power down mode. [PDEN] do not disable DLL.

Self-refresh exit [SELFX]: This command is executed to exit from self-refresh mode. 10 cycles (= t_{SNR}) after [SELFX], non-read commands can be executed. For read operation, wait for 200 cycles (= t_{SRD}) after [SELFX] to adjust Dout timing by DLL. After the exit, within 7.8 µs input auto-refresh command.

Power down exit [PDEX]: The DDR SDRAM can exit from power down mode t_{PDEX} (1 cycle min.) after the cycle when [PDEX] is issued.

Function Truth Table

The following tables show the operations that are performed when each command is issued in each state of the DDR SDRAM.

Function Truth Table (1)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation	Next state
Precharging*[2]	H	×	×	×	×	DESL	NOP	Idle
	L	H	H	H	×	NOP	NOP	Idle
	L	H	H	L	×	BST	ILLEGAL*[12]	—
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL*[12]	—
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL*[12]	—
	L	L	H	H	BA, RA	ACTV	ILLEGAL*[12]	—
	L	L	H	L	BA, A10	PRE, PALL	NOP	Idle
	L	L	L	×	×		ILLEGAL	—
Idle*[3]	H	×	×	×	×	DESL	NOP	Idle
	L	H	H	H	×	NOP	NOP	Idle
	L	H	H	L	×	BST	ILLEGAL*[12]	—
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL*[12]	—
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL*[12]	—
	L	L	H	H	BA, RA	ACTV	ILLEGAL*[12]	Activating
	L	L	H	L	BA, A10	PRE, PALL	NOP	Idle
	L	L	L	H	×	REF, SELF	Refresh/ Selfrefresh*[13]	Idle/ Selfrefresh
	L	L	L	L	MODE	MRS	Mode register set*[13]	Idle
Refresh (auto-refresh)*[4]	H	×	×	×	×	DESL	NOP	Idle
	L	H	H	H	×	NOP	NOP	Idle
	H	H	H	L	×	BST	ILLEGAL	—
	L	H	L	×	×		ILLEGAL	—
	L	L	×	×	×		ILLEGAL	—

Function Truth Table (2)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation	Next state
Activating*[5]	H	×	×	×	×	DESL	NOP	Active
	L	H	H	H	×	NOP	NOP	Active
	L	H	H	L	×	BST	ILLEGAL*[12]	—
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL*[12]	—
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL*[12]	—
	L	L	H	H	BA, RA	ACTV	ILLEGAL*[12]	—
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL*[12]	—
	L	L	L	×	×		ILLEGAL	—
Active*[6]	H	×	×	×	×	DESL	NOP	Active
	L	H	H	H	×	NOP	NOP	Active
	L	H	H	L	×	BST	ILLEGAL	Active
	L	H	L	H	BA, CA, A10	READ/READA	Starting read operation	Read/READA
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Starting write operation	Write recovering/ precharging
	L	L	H	H	BA, RA	ACTV	ILLEGAL*[12]	—
	L	L	H	L	BA, A10	PRE, PALL	Pre-charge	Idle
	L	L	L	×	×		ILLEGAL	—
Read*[7]	H	×	×	×	×	DESL	NOP	Active
	L	H	H	H	×	NOP	NOP	Active
	L	H	H	L	×	BST	BST	Active
	L	H	L	H	BA, CA, A10	READ/READA	Interrupting burst read operation to start new read	Active
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL*[14]	—
	L	L	H	H	BA, RA	ACTV	ILLEGAL*[12]	—
	L	L	H	L	BA, A10	PRE, PALL	Interrupting burst read operation to start pre-charge	Precharging
	L	L	L	×	×		ILLEGAL	—

Function Truth Table (3)

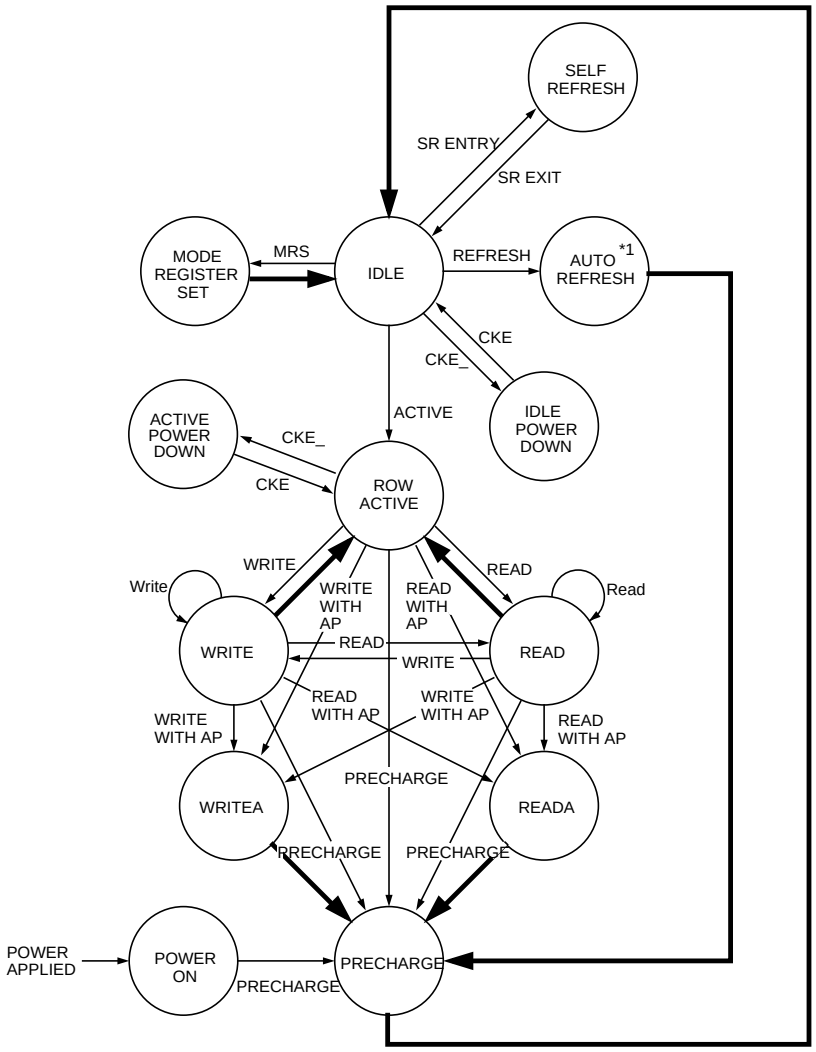
Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation	Next state
Read with auto-pre-charge*[8]	H	×	×	×	×	DESL	NOP	Precharging
	L	H	H	H	×	NOP	NOP	Precharging
	L	H	H	L	×	BST	ILLEGAL	—
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	—
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	—
	L	L	H	H	BA, RA	ACTV	ILLEGAL*[12]	—
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL*[12]	—
	L	L	L	×	×		ILLEGAL	—
Write*[9]	H	×	×	×	×	DESL	NOP	Write recovering
	L	H	H	H	×	NOP	NOP	Write recovering
	L	H	H	L	×	BST	ILLEGAL	—
	L	H	L	H	BA, CA, A10	READ/READA	Interrupting burst write operation to start read operation.	Read/ReadA
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Interrupting burst write operation to start new write operation.	Write/WriteA
	L	L	H	H	BA, RA	ACTV	ILLEGAL*[12]	—
	L	L	H	L	BA, A10	PRE, PALL	Interrupting write operation to start pre-charge.	Idle
	L	L	L	×	×		ILLEGAL	—
Write recovering*[10]	H	×	×	×	×	DESL	NOP	Active
	L	H	H	H	×	NOP	NOP	Active
	L	H	H	L	×	BST	ILLEGAL	—
	L	H	L	H	BA, CA, A10	READ/READA	Starting read operation.	Read/ReadA
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Starting new write operation.	Write/WriteA
	L	L	H	H	BA, RA	ACTV	ILLEGAL*[12]	—
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL*[12]	—
	L	L	L	×	×		ILLEGAL	—

Function Truth Table (4)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation	Next state
Write with auto-pre-charge*[11]	H	×	×	×	×	DESL	NOP	Precharging
	L	H	H	H	×	NOP	NOP	Precharging
	L	H	H	L	×	BST	ILLEGAL	—
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	—
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL	—
	L	L	H	H	BA, RA	ACTV	ILLEGAL*[12]	—
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL*[12]	—
	L	L	L	×	×		ILLEGAL	—

Notes: 1. H: V_{IH}. L: V_{IL}. ×: V_{IH} or V_{IL}.
2. The DDR SDRAM is in "Precharging" state for t_{RP} after precharge command is issued.
3. The DDR SDRAM reachs "IDLE" state t_{RP} after precharge command is issued.
4. The DDR SDRAM is in "Refresh" state for t_{RC} after auto-refresh command is issued.
5. The DDR SDRAM is in "Activating" state for t_{RCD} after ACTV command is issued.
6. The DDR SDRAM is in "Active" state after "Activating" is completed.
7. The DDR SDRAM is in "READ" state until burst data have been output and DQ output circuits are turned off.
8. The DDR SDRAM is in "READ with auto-precharge" from READA command until burst data has been output and DQ output circuits are turned off.
9. The DDR SDRAM is in "WRITE" state from WRIT command to the last burst data are input.
10. The DDR SDRAM is in "Write recovering" for t_{WR} after the last data are input.
11. The DDR SDRAM is in "Write with auto-precharge" until t_{WR} after the last data has been input.
12. This command may be issued for other banks, depending on the state of the banks.
13. All banks must be in "IDLE".
14. Before executing a write command to stop the preceding burst read operation, BST command must be issued.

Simplified State Diagram



Automatic transition after completion of command.
Transition resulting from command input.

Note: 1. After the auto-refresh operation, precharge operation is performed automatically and enter the IDLE state.

Operation of the DDR SDRAM

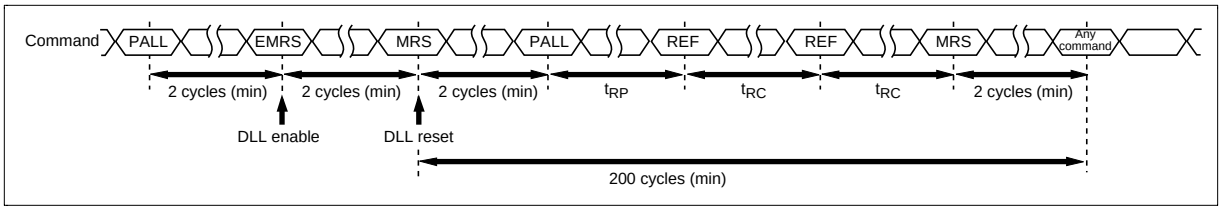
Power-up Sequence

The following sequence is recommended for Power-up.

(1) Apply power and attempt to maintain CKE at an LVCMOS low state (all other inputs may be undefined).
Apply V_{CC} before or at the same time as V_{CCQ}.
Apply V_{CCQ} before or at the same time as V_{TT} and V_{REF}.
(2) Start clock and maintain stable condition for a minimum of 200 μs.
(3) After the minimum 200 μs of stable power and clock (CLK, $\overline{CLK}$), apply NOP and take CKE high.
(4) Issue precharge all command for the device.
(5) Issue EMRS to enable DLL.
(6) Issue a mode register set command (MRS) for "DLL reset" with bit A8 set to high (An additional 200 cycles of clock input is required to lock the DLL after every DLL reset).
(7) Issue precharge all command for the device.*[1]
(8) Issue 2 or more auto-refresh commands.*[1]
(9) Issue a mode register set command to initialize device operation.

Note: 1. Sequence of (7) and (8) may be reversed.

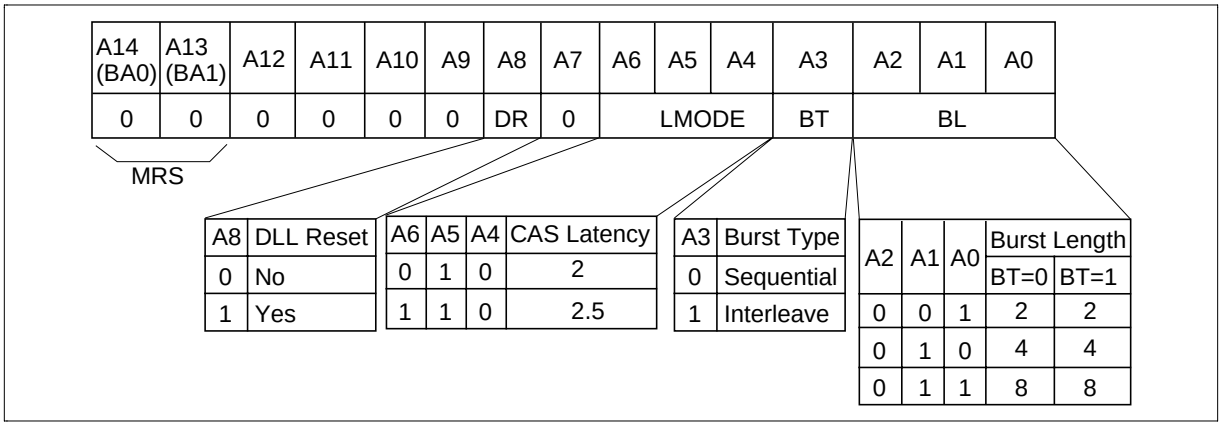
Power-up Sequence after CKE Goes High



Mode Register and Extended Mode Register Set

There are two mode registers, the mode register and the extended mode register so as to define the operating mode. Parameters are set to both through the A0 to the A14 pins by the mode register set command [MRS] or the extended mode register set command [EMRS]. The mode register and the extended mode register are set by inputting signal via the A0 to the A14 during mode register set cycles. A14 (BA0) and A13 (BA1) determine which one of the mode register or the extended mode register are set. Prior to a read or a write operation, the mode register must be set.
Remind that no other parameters are shown in the table bellow are allowed to input to the registers.

Mode Register Set [MRS] (A14 = 0, A13 = 0)



A14 (BA0)	A13 (BA1)	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	0	DR	0	LMODE			BT	BL		

MRS

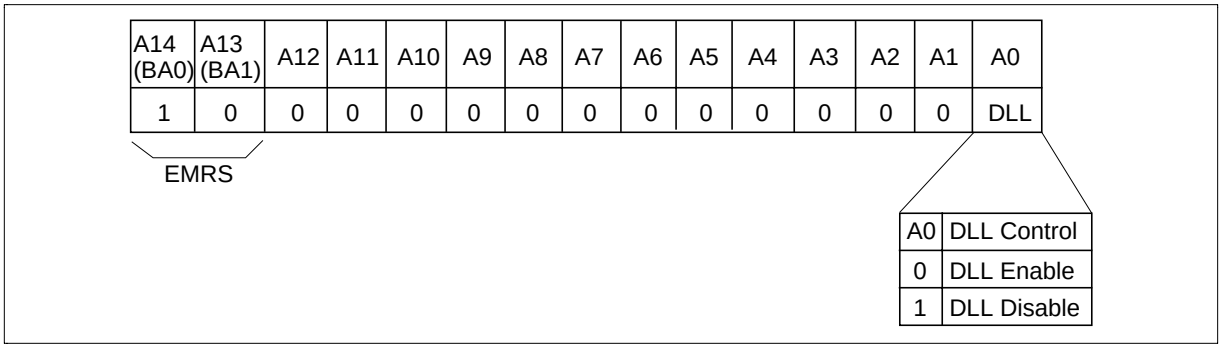
A8	DLL Reset
0	No
1	Yes

A6	A5	A4	CAS Latency
0	1	0	2
1	1	0	2.5

A3	Burst Type
0	Sequential
1	Interleave

A2	A1	A0	Burst Length	
			BT=0	BT=1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8

Extended Mode Register Set [EMRS] (A14 = 1, A13 = 0)



A14 (BA0)	A13 (BA1)	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	DLL

EMRS

A0	DLL Control
0	DLL Enable
1	DLL Disable

Burst Operation

The burst type (BT) and the first three bits of the column address determines the order of a data out.

Burst length = 2

Starting Ad.	Addressing(decimal)	
A0	Sequence	Interleave
0	0, 1,	0, 1,
1	1, 0,	1, 0,

Burst length = 4

Starting Ad.		Addressing(decimal)	
A1	A0	Sequence	Interleave
0	0	0, 1, 2, 3,	0, 1, 2, 3,
0	1	1, 2, 3, 0,	1, 0, 3, 2,
1	0	2, 3, 0, 1,	2, 3, 0, 1,
1	1	3, 0, 1, 2,	3, 2, 1, 0,

Burst length = 8

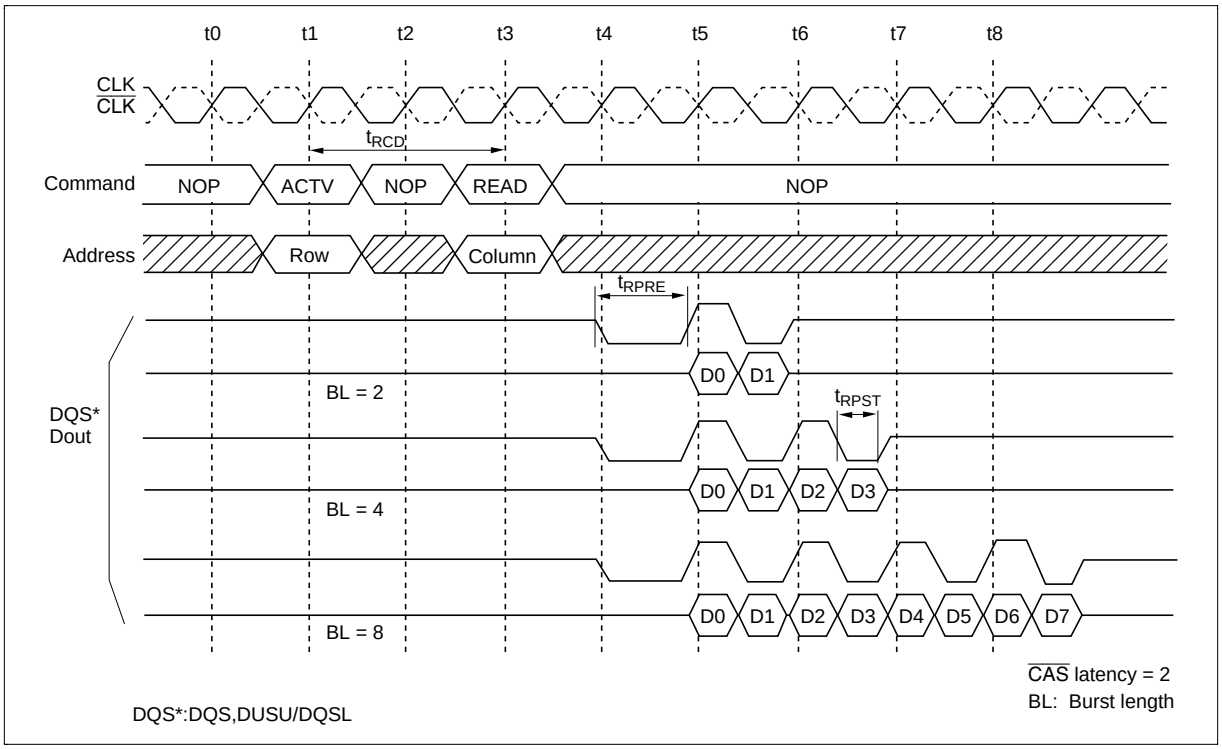
Starting Ad.			Addressing(decimal)	
A2	A1	A0	Sequence	Interleave
0	0	0	0, 1, 2, 3, 4, 5, 6, 7,	0, 1, 2, 3, 4, 5, 6, 7,
0	0	1	1, 2, 3, 4, 5, 6, 7, 0,	1, 0, 3, 2, 5, 4, 7, 6,
0	1	0	2, 3, 4, 5, 6, 7, 0, 1,	2, 3, 0, 1, 6, 7, 4, 5,
0	1	1	3, 4, 5, 6, 7, 0, 1, 2,	3, 2, 1, 0, 7, 6, 5, 4,
1	0	0	4, 5, 6, 7, 0, 1, 2, 3,	4, 5, 6, 7, 0, 1, 2, 3,
1	0	1	5, 6, 7, 0, 1, 2, 3, 4,	5, 4, 7, 6, 1, 0, 3, 2,
1	1	0	6, 7, 0, 1, 2, 3, 4, 5,	6, 7, 4, 5, 2, 3, 0, 1,
1	1	1	7, 0, 1, 2, 3, 4, 5, 6,	7, 6, 5, 4, 3, 2, 1, 0,

Read/Write Operations

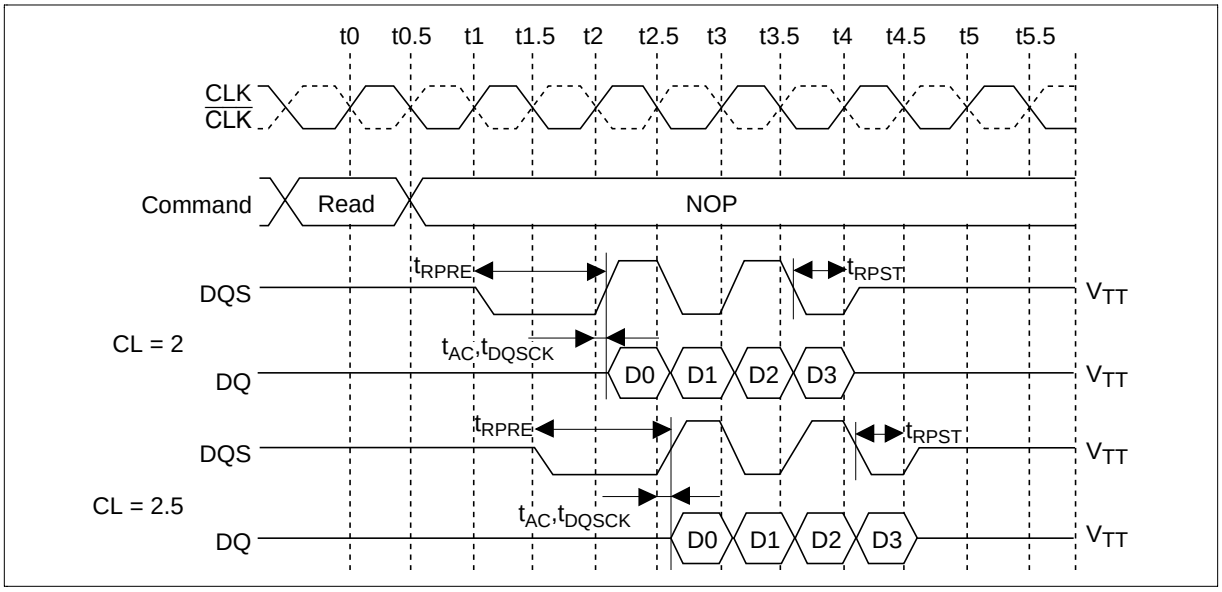
Bank active: A read or a write operation begins with the bank active command [ACTV]. The bank active command determines a bank address (AX14, AX13) and a row address (AX0 to AX12). For the bank and the row, a read or a write command can be issued t_{RCD} after the ACTV is issued.

Read operation: The burst length (BL), the $\overline{CAS}$ latency (CL) and the burst type (BT) of the mode register are referred when a read command is issued. The burst length (BL) determines the length of a sequential output data by the read command which can be set to 2, 4, or 8. The starting address of the burst read is defined by the column address (AY0 to AY8; the HM5425161B, AY0 to AY9; the HM5425801B, AY0 to AY9, AY11; the HM5425401B), the bank select address (AX14, AX13) which are loaded via the A0 to A14 pins in the cycle when the read command is issued. The data output timing are characterized by CL (2 or 2.5) and t_{AC}. The read burst start CL • t_{CK} + t_{AC} (ns) after the clock rising edge where the read command are latched. The DDR SDRAM output the data strobe through DQS or DQSU/DQSL simultaneously with data. t_{RPRE} prior to the first rising edge of the data strobe, the DQS or the DQSU/DQSL are driven Low from V_{TT} level. This low period of DQS is referred as read preamble. The burst data are output coincidentally at both the rising and falling edge of the data strobe. The DQ pins become High-Z in the next cycle after the burst read operation completed. t_{RPST} from the last falling edge of the data strobe, the DQS pins become High-Z. This low period of DQS is referred as read postamble.

Read Operation (Burst Length)

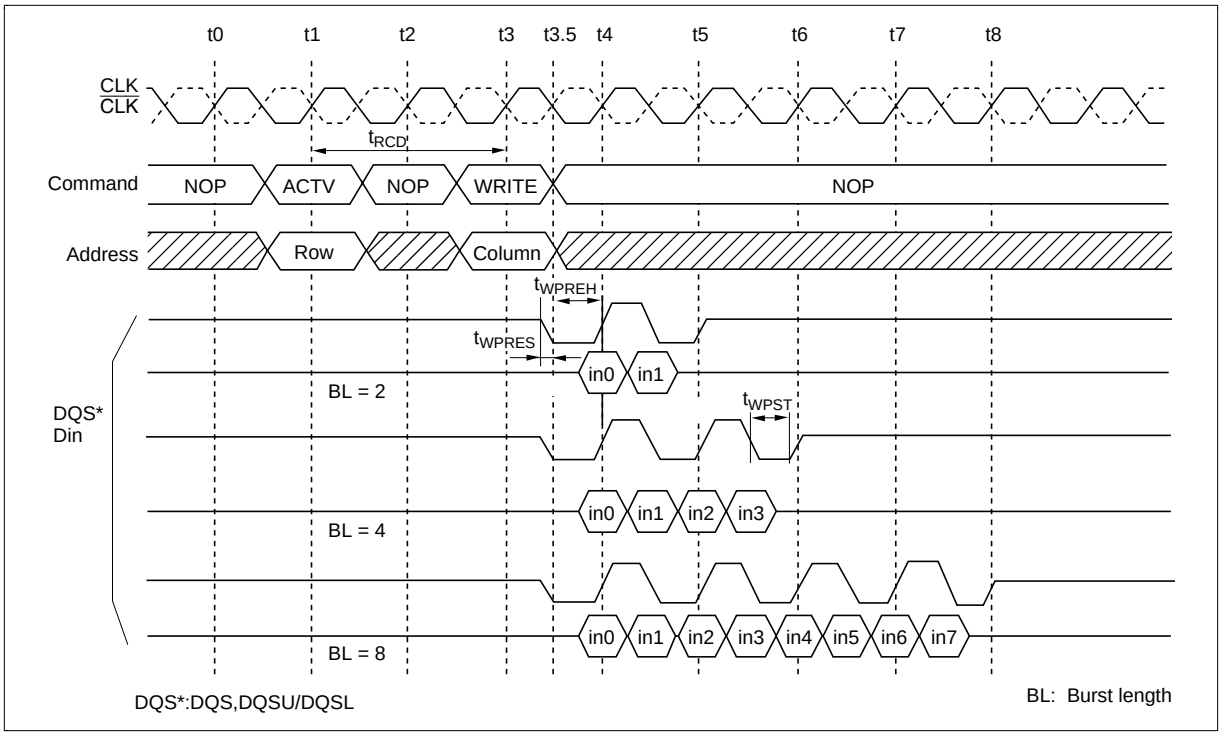


Read Operation ($\overline{\text{CAS}}$ Latency)



Write operation: The burst length (BL) and the burst type (BT) of the mode register are referred when a write command is issued. The burst length (BL) determines the length of a sequential data input by the write command which can be set to 2, 4, or 8. The latency from write command to data input is fixed to 1. The starting address of the burst read is defined by the column address (AY0 to AY8; the HM5425161B, AY0 to AY9; the HM5425801B, AY0 to AY9, AY11; the HM5425401B), the bank select address (AX14, AX13) which are loaded via the A0 to A14 pins in the cycle when the write command is issued. DQS, DQSU/DQSL should be input as the strobe for the input-data and DM, DMU/DML as well during burst operation. t_{WPREH} prior to the first rising edge of the DQS, the DQSU/DQSL should be set to Low and t_{WPST} after the last falling edge of the data strobe can be set to High-Z. The leading low period of DQS is referred as write preamble. The last low period of DQS is referred as wrtie postamble.

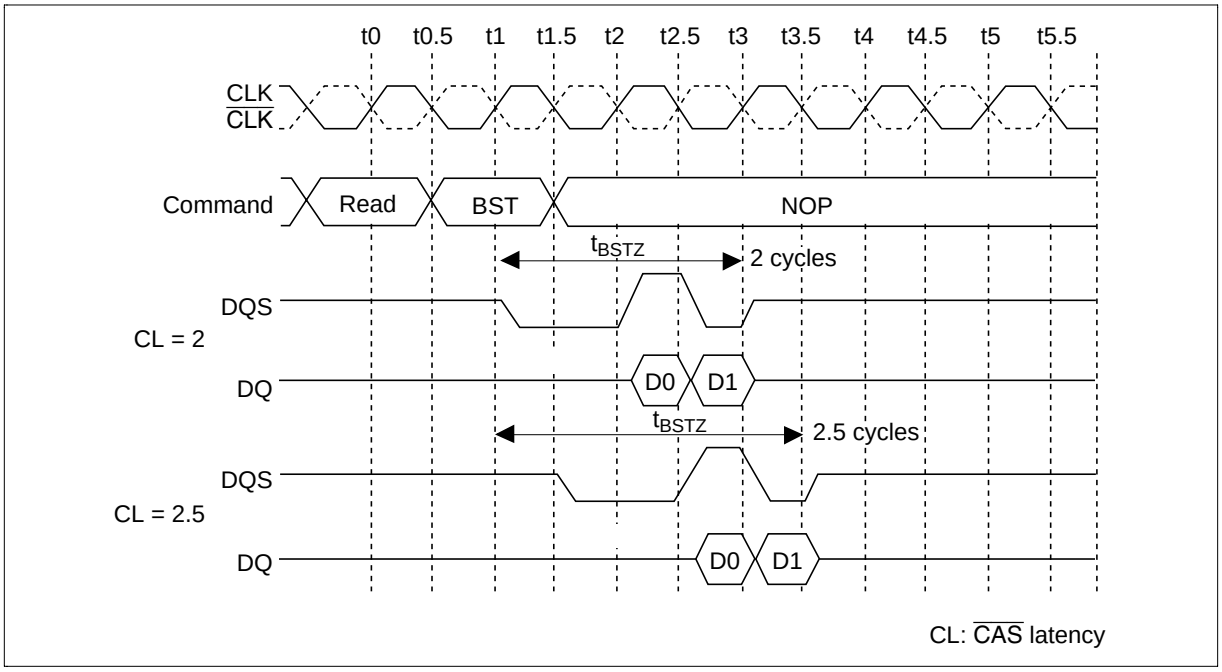
Write Operation



Burst Stop

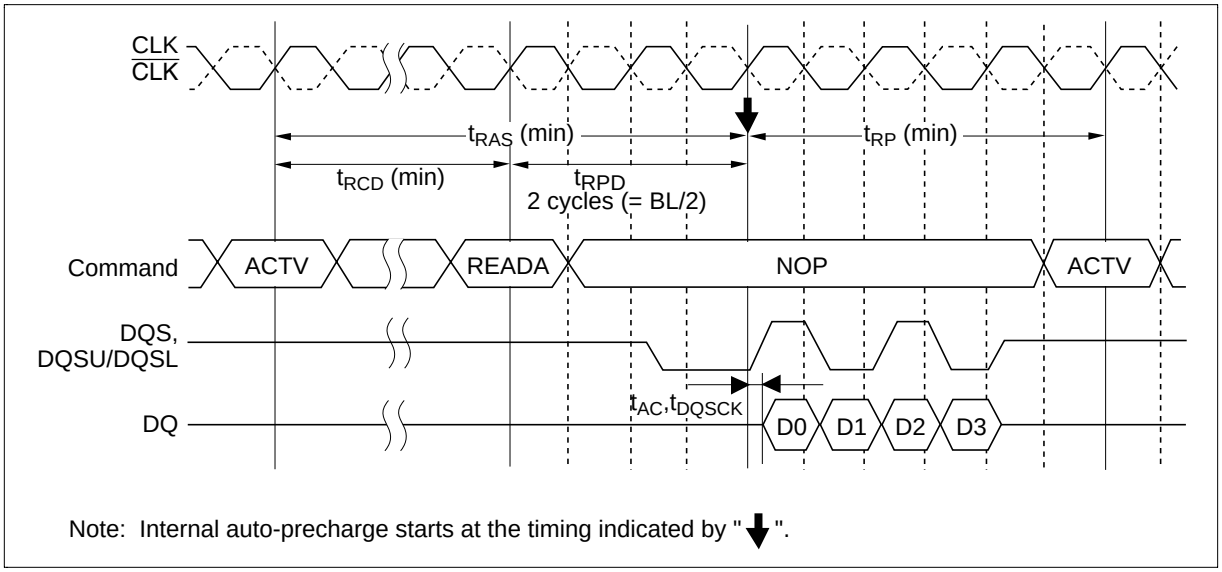
Burst stop command during burst read: The burst stop (BST) command is used to stop data output during a burst read. The BST command stops the burst read and sets the output buffer to High-Z. t_{BSTZ} (= CL) cycles after a BST command issued, the DQ pins become High-Z. The BST command is not supported for the burst write operation. Note that bank address is not referred when this command is executed.

Burst Stop during a Read Operation



Auto Precharge

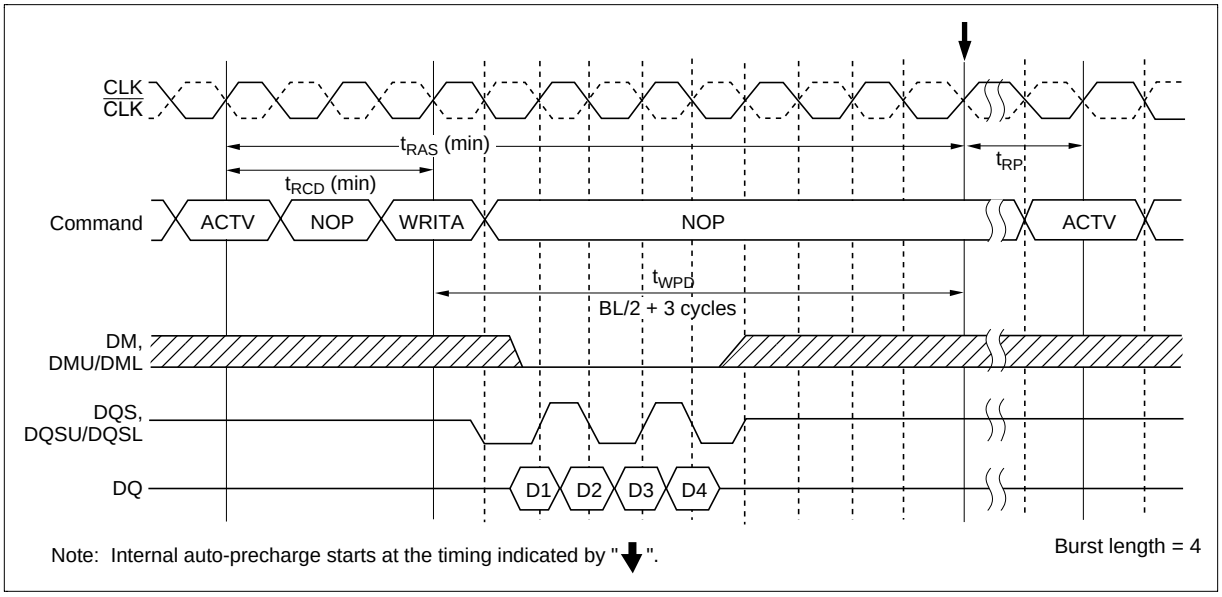
Read with auto-precharge: The precharge is automatically performed after completing a read operation. The precharge starts t_{RPD} (BL/2) cycle after READA command input. t_{RCD} for READA should be determined so that t_{RC} (ACTV to ACTV) spec. is obeyed when READA is issued successively after a bank active command, that is t_{RCD} (READA) ≥ t_{RC} (min.)-t_{RP} (min.)-t_{RPD}. A column command to the other active bank can be issued the next cycle after the last data output. Read with auto-precharge command does not limit row commands execution for other bank.



Note: Internal auto-precharge starts at the timing indicated by "↓".

Write with auto-precharge: The precharge is automatically performed after completing a burst write operation. The precharge operation is started t_{WPD} (= BL/ 2 + 3) cycles after WRITA command issued. t_{RCD} for WRITA should be determined so that t_{RC} (ACTV to ACTV) spec. is obeyed when WRITA is issued successively after a bank active command, that is t_{RCD} (WRITA) ≥ t_{RC}(min.)-t_{RP}(min.)-t_{WPD}. A column command to the other active command can be issued the next cycle after the internal precharge command issued. Write with auto-precharge command does not limit row commands execution for other bank.

Burst Write (Burst Length = 4)

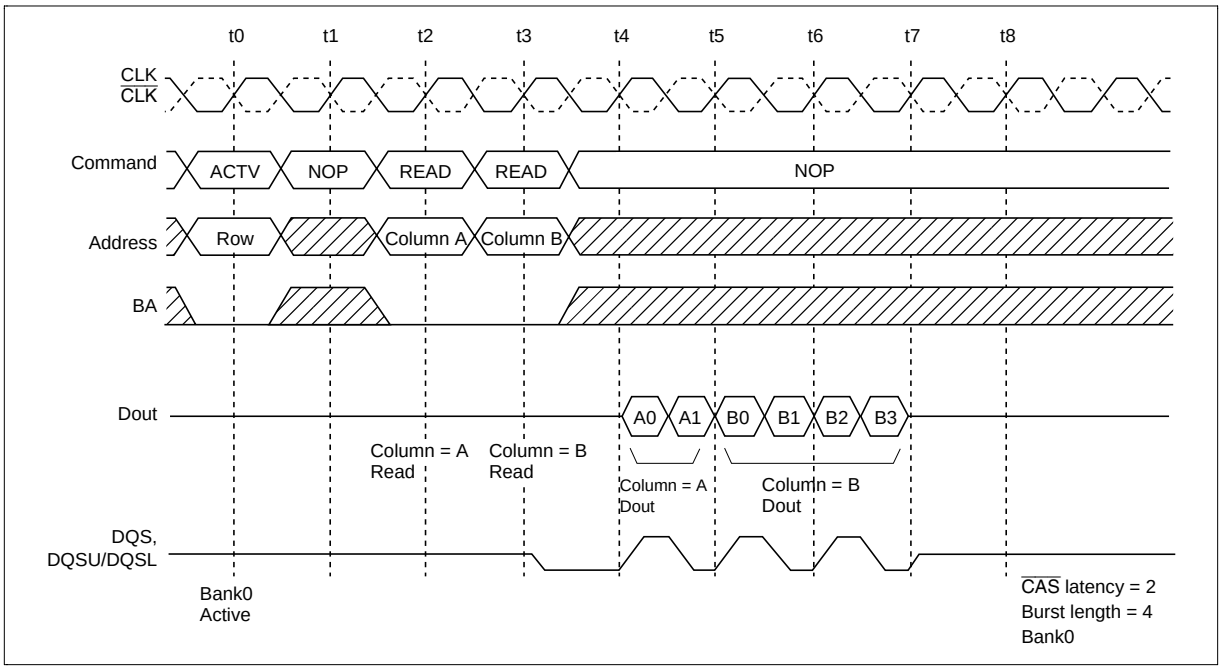


Command Intervals

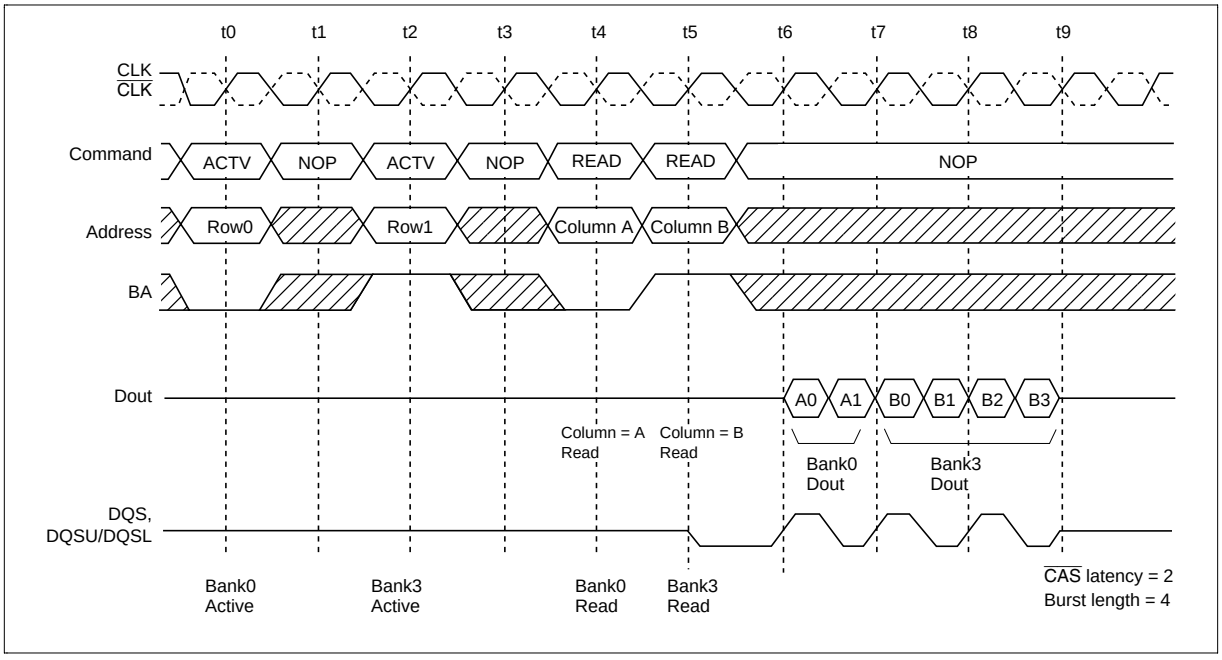
A Read command to the consecutive Read command Interval

	Destination row of the consecutive read command			
	Bank address	**Row address**	**State**	**Operation**
1.	Same	Same	ACTIVE	The consecutive read can be performed after an interval of no less than 1 cycle to interrupt the preceding read operation.
2.	Same	Different	—	Precharge the bank to interrupt the preceding read operation. t_{RP} after the precharge command, issue the ACTV command. t_{RCD} after the ACTV command, the consecutive read command can be issued. See 'A read command to the consecutive precharge interval' section.
3.	Different	Any	ACTIVE	The consecutive read can be performed after an interval of no less than 1 cycle to interrupt the preceding read operation.
			IDLE	Precharge the bank without interrupting the preceding read operation. t_{RP} after the precharge command, issue the ACTV command. t_{RCD} after the ACTV command, the consecutive read command can be issued.

READ to READ Command Interval (same ROW address in the same bank)



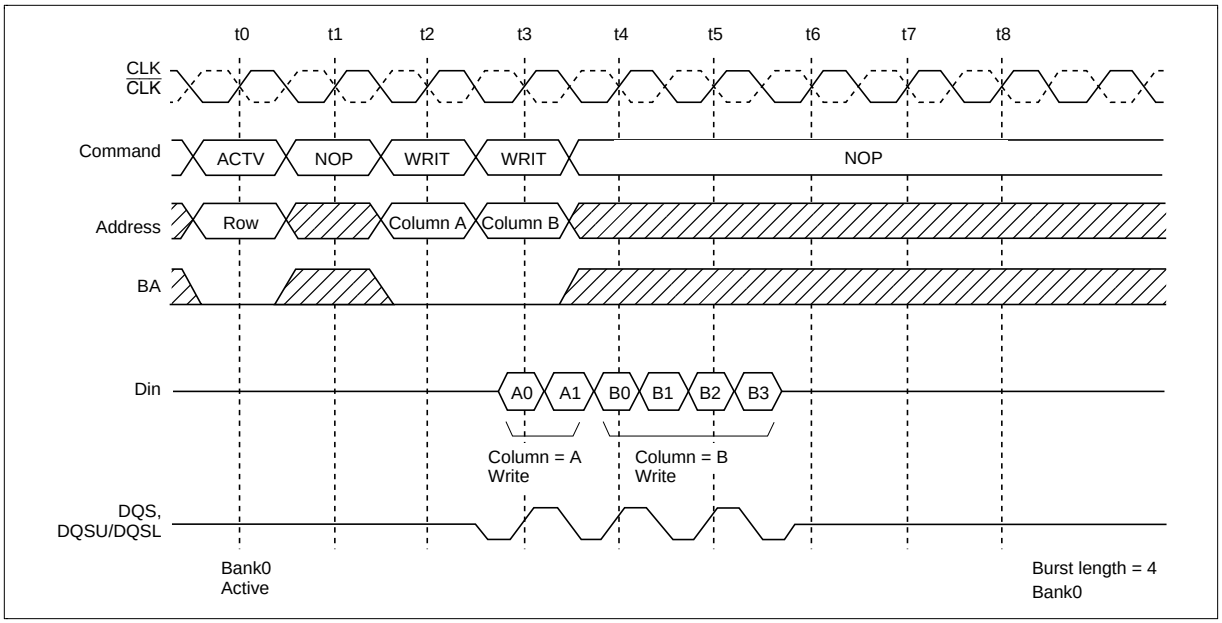
READ to READ Command Interval (different bank)



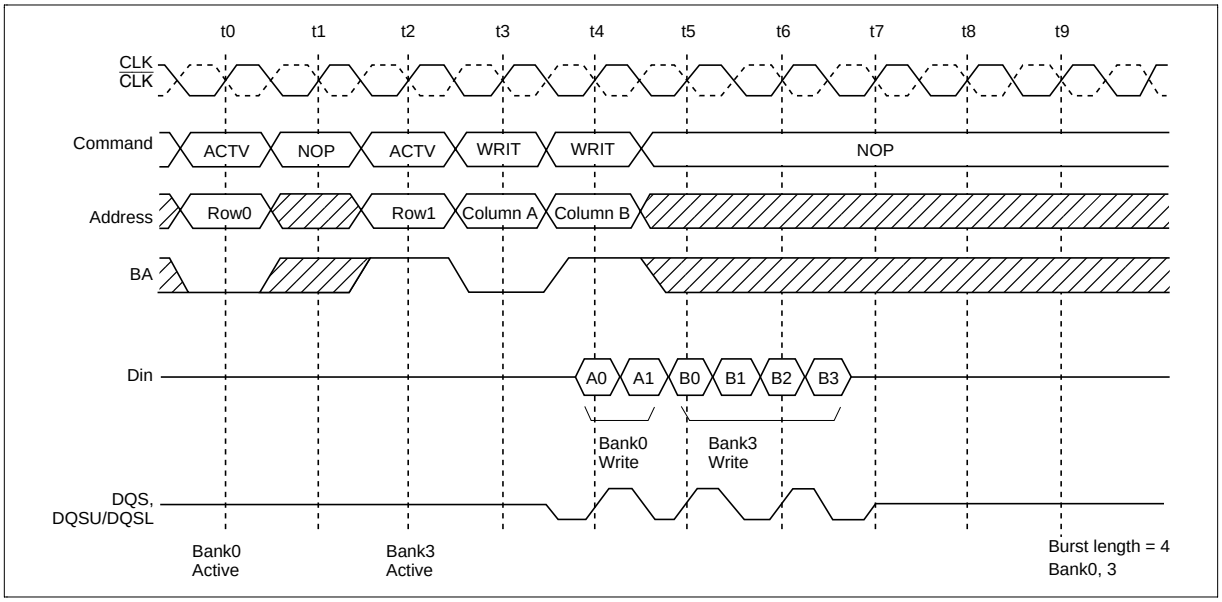
A Write command to the consecutive Write command Interval:

	Destination row of the consecutive write command			
	Bank address	**Row address**	**State**	**Operation**
1.	Same	Same	ACTIVE	The consecutive write can be performed after an interval of no less than 1 cycle to interrupt the preceding write operation.
2.	Same	Different	—	Precharge the bank to interrupt the preceding write operation. t_{RP} after the precharge command, issue the ACTV command. t_{RCD} after the ACTV command, the consecutive write command can be issued. See 'A write command to the consecutive precharge interval' section.
3.	Different	Any	ACTIVE	The consecutive write can be performed after an interval of no less than 1 cycle to interrupt the preceding write operation.
			IDLE	Precharge the bank without interrupting the preceding write operation. t_{RP} after the precharge command, issue the ACTV command. t_{RCD} after the ACTV command, the consecutive write command can be issued.

WRITE to WRITE Command Interval (same ROW address in the same bank)



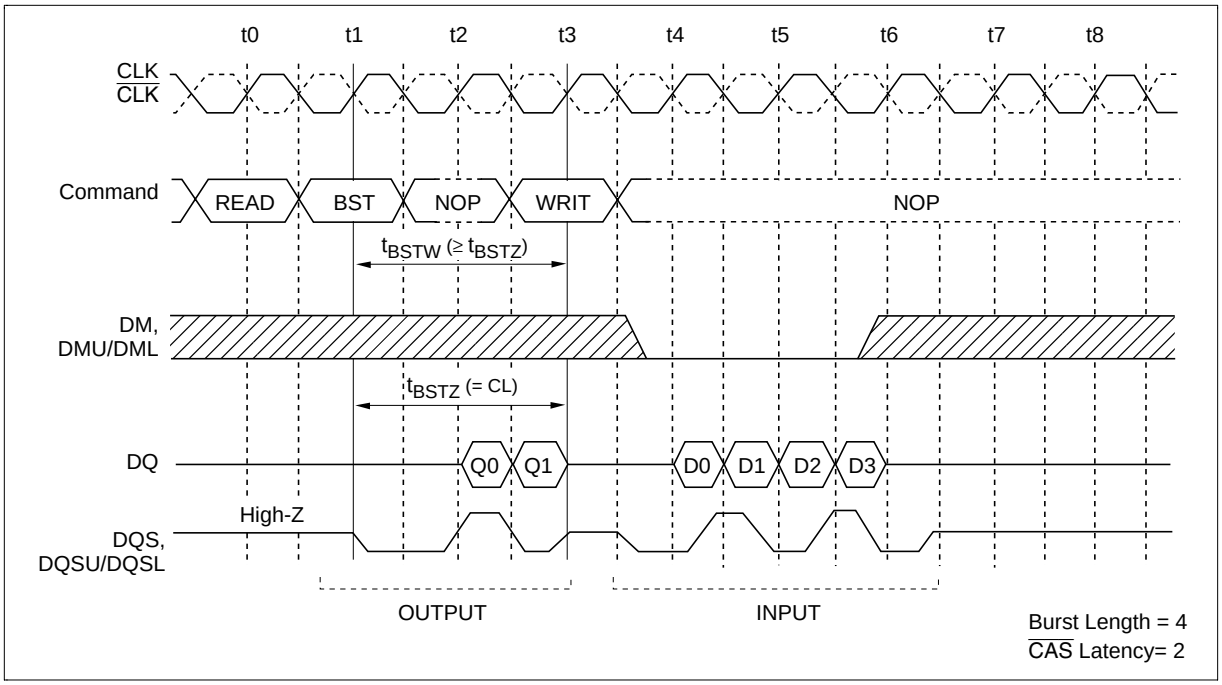
WRITE to WRITE Command Interval (different bank)



A Read command to the consecutive Write command interval with the BST command

	Destination row of the consecutive write command			
	Bank address	**Row address**	**State**	**Operation**
1.	Same	Same	ACTIVE	Issue the BST command. t_{BSTW} ($\geq t_{BSTZ}$) after the BST command, the consecutive write command can be issued.
2.	Same	Different	—	Precharge the bank to interrupt the preceding read operation. t_{RP} after the precharge command, issue the ACTV command. t_{RCD} after the ACTV command, the consecutive write command can be issued. See 'A read command to the consecutive precharge interval' section.
3.	Different	Any	ACTIVE	Issue the BST command. t_{BSTW} ($\geq t_{BSTZ}$) after the BST command, the consecutive write command can be issued.
			IDLE	Precharge the bank independently of the preceding read operation. t_{RP} after the precharge command, issue the ACTV command. t_{RCD} after the ACTV command, the consecutive write command can be issued.

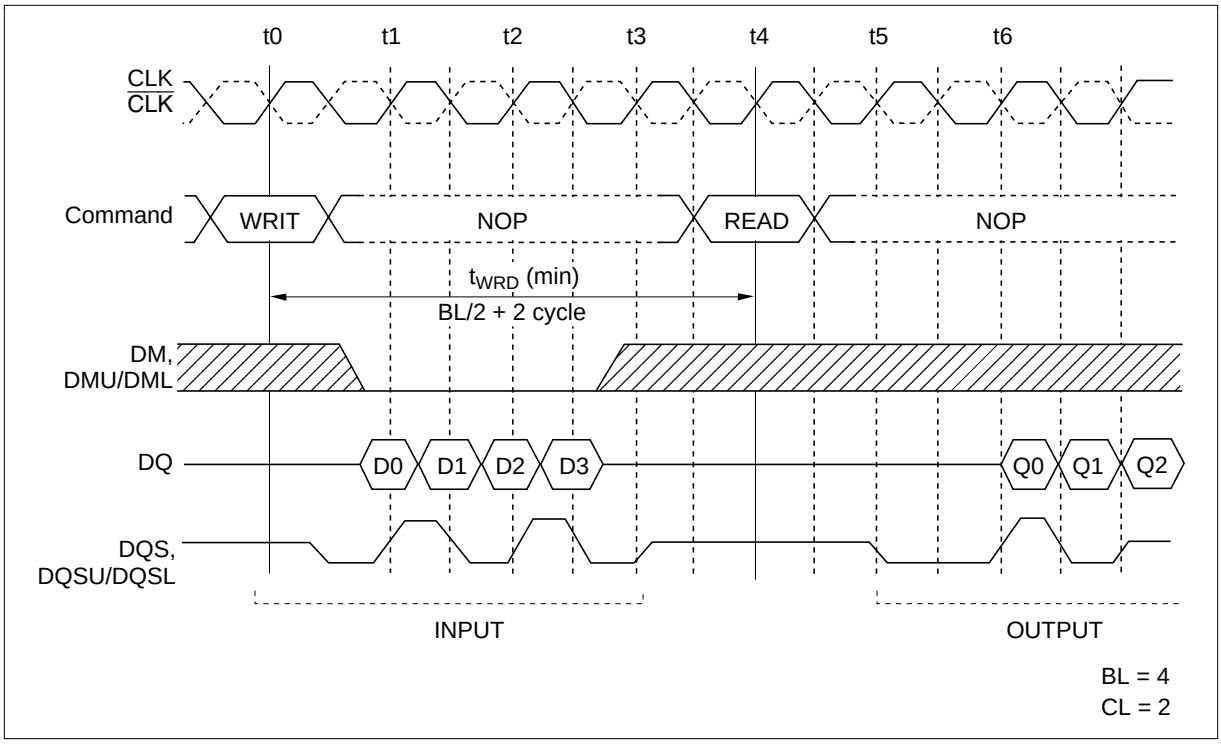
READ to WRITE Command Interval



A Write command to the consecutive Read command interval: To complete the burst operation

	Destination row of the consecutive read command			
	Bank address	**Row address**	**State**	**Operation**
1.	Same	Same	ACTIVE	To complete the burst operation, the consecutive read command should be performed t_{WRD} (= BL/ 2 + 2) after the write command.
2.	Same	Different	—	Precharge the bank t_{WRD} after the preceding write command. t_{RP} after the precharge command, issue the ACTV command. t_{RCD} after the ACTV command, the consecutive read command can be issued. See 'A read command to the consecutive precharge interval' section.
3.	Different	Any	ACTIVE	To complete a burst operation, the consecutive read command should be performed t_{WRD} (= BL/ 2 + 2) after the write command.
			IDLE	Precharge the bank independently of the preceding write operation. t_{RP} after the precharge command, issue the ACTV command. t_{RCD} after the ACTV command, the consecutive read command can be issued.

WRITE to READ Command Interval



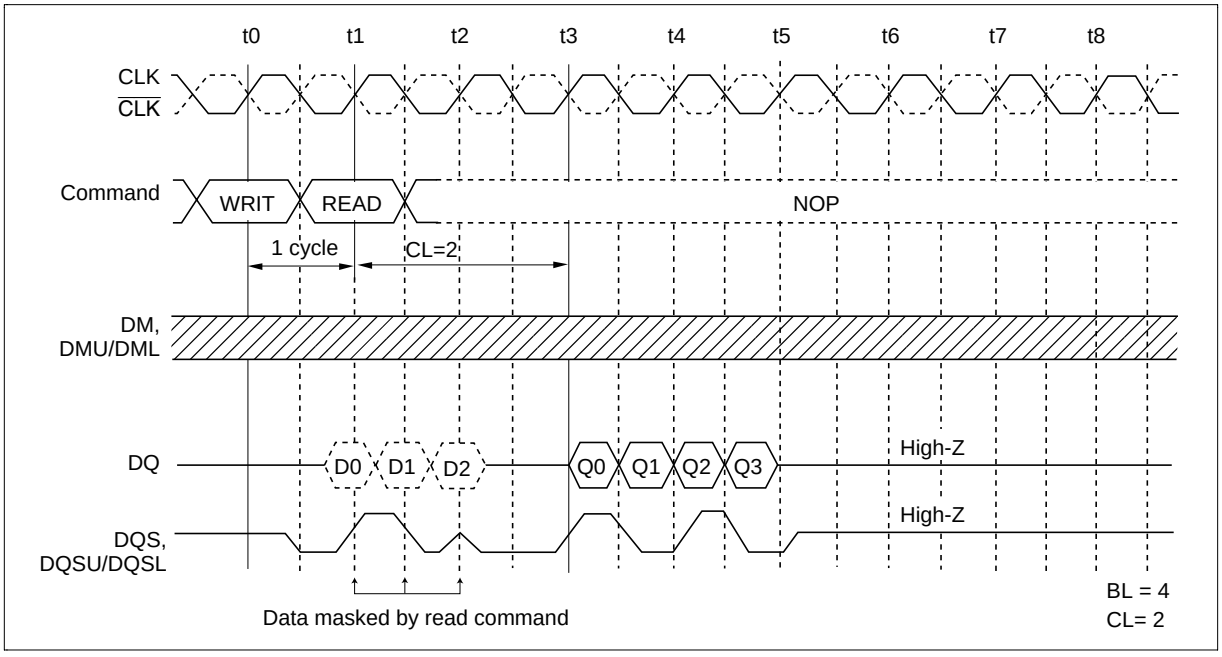
A Write command to the consecutive Read command interval: To interrupt the write operation

	Destination row of the consecutive read command			
	Bank address	**Row address**	**State**	**Operation**
1.	Same	Same	ACTIVE	DM, DMU/DML must be input 1 cycle prior to the read command input to prevent from being written invalid data. In case, the read command is input in the next cycle of the write command, DM, DMU/DML is not necessary.
2.	Same	Different	—	—*1
3.	Different	Any	ACTIVE	DM, DMU/DML must be input 1 cycle prior to the read command input to prevent from being written invalid data. In case, the read command is input in the next cycle of the write command, DM, DMU/DML is not necessary.
			IDLE	—*1

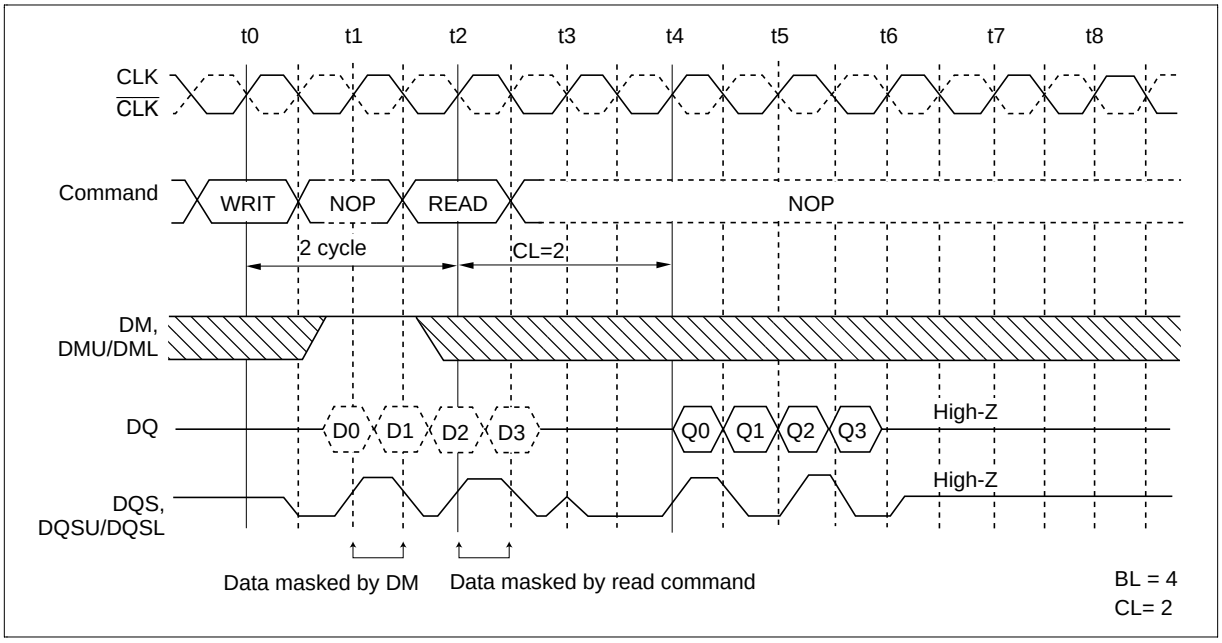
Note: 1. Precharge must be preceded to read command. Therefore read command can not interrupt the write operation in this case.

WRITE to READ Command Interval (Samebank, same ROW address)

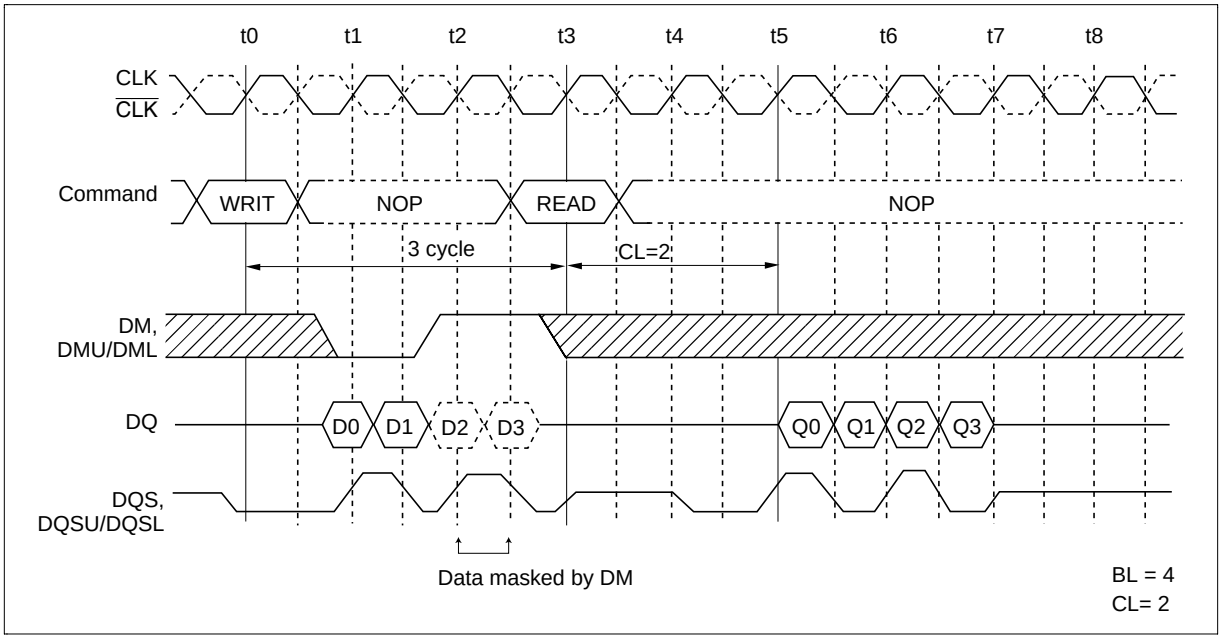
[WRITE to READ delay = 1 clock cycle]



[**WRITE to READ delay = 2 clock cycle]**



[**WRITE to READ delay = 3 clock cycle]**

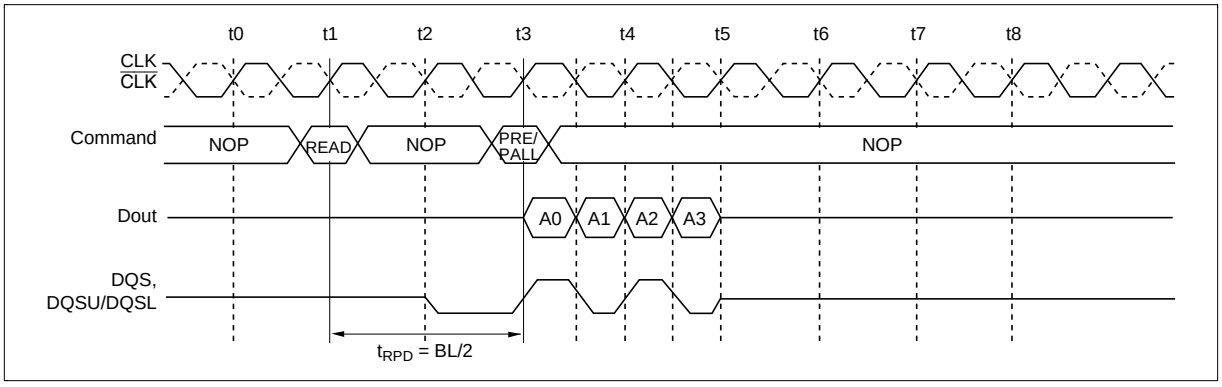


A Read command to the consecutive Precharge command interval (same bank):

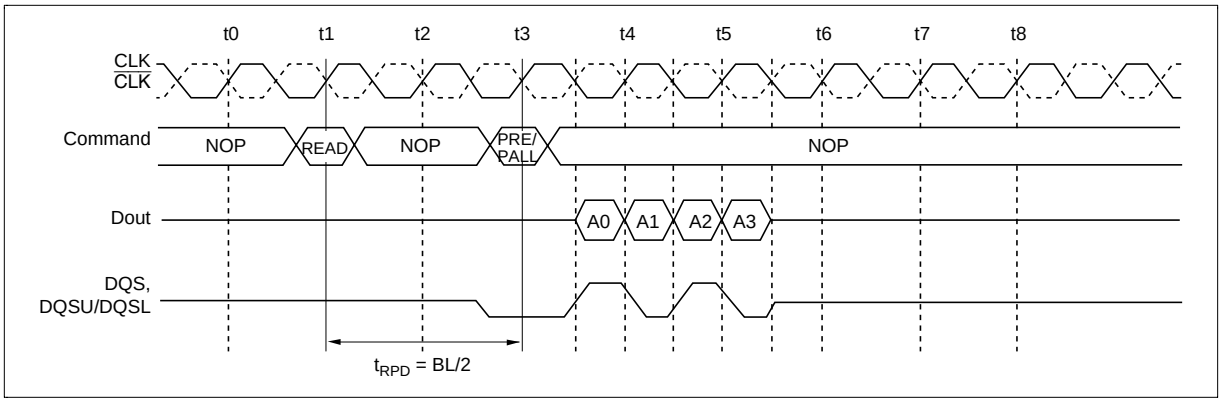
To output all data: To complete a burst read opeartion and get a burst length of data, the consecutive precharge command must be issued t_{RPD} (= BL/ 2 cycles) after the read command is issued.

READ to PRECHARGE Command Interval (same bank): To output all data

$\overline{CAS}$ Latency = 2, Burst Length = 4



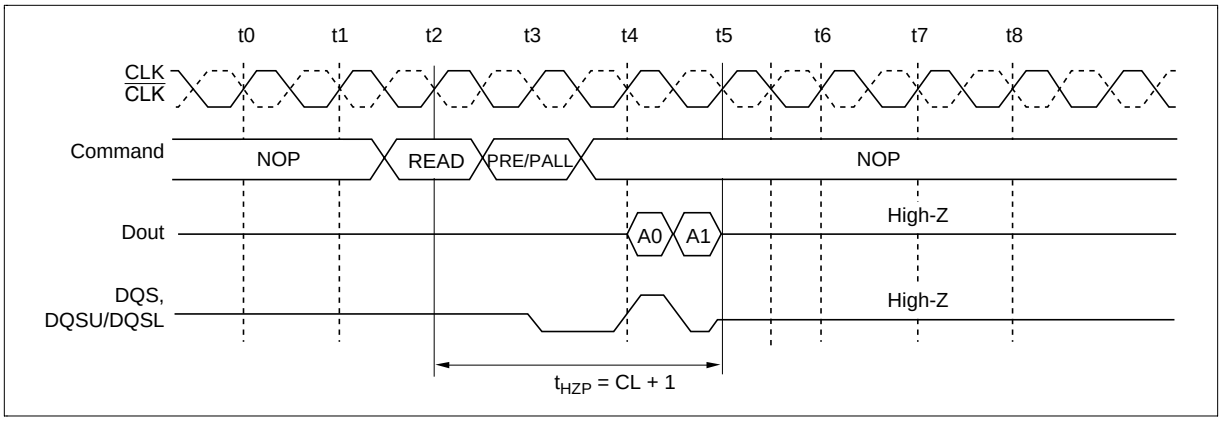
$\overline{CAS}$ Latency = 2.5, Burst Length = 4



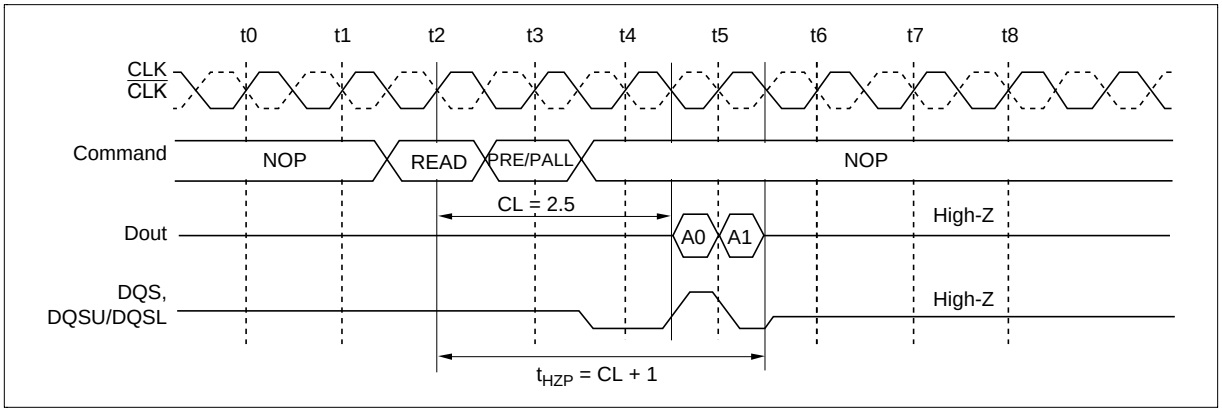
READ to PRECHARGE Command Interval (same bank): To stop output data

A burst data output can be interrupted with a precharge command. All DQ pins and DQS pins become High-Z t_{HZP} (= CL) after the precharge command.

$\overline{CAS}$ Latency = 2, Burst Length = 2, 4, 8



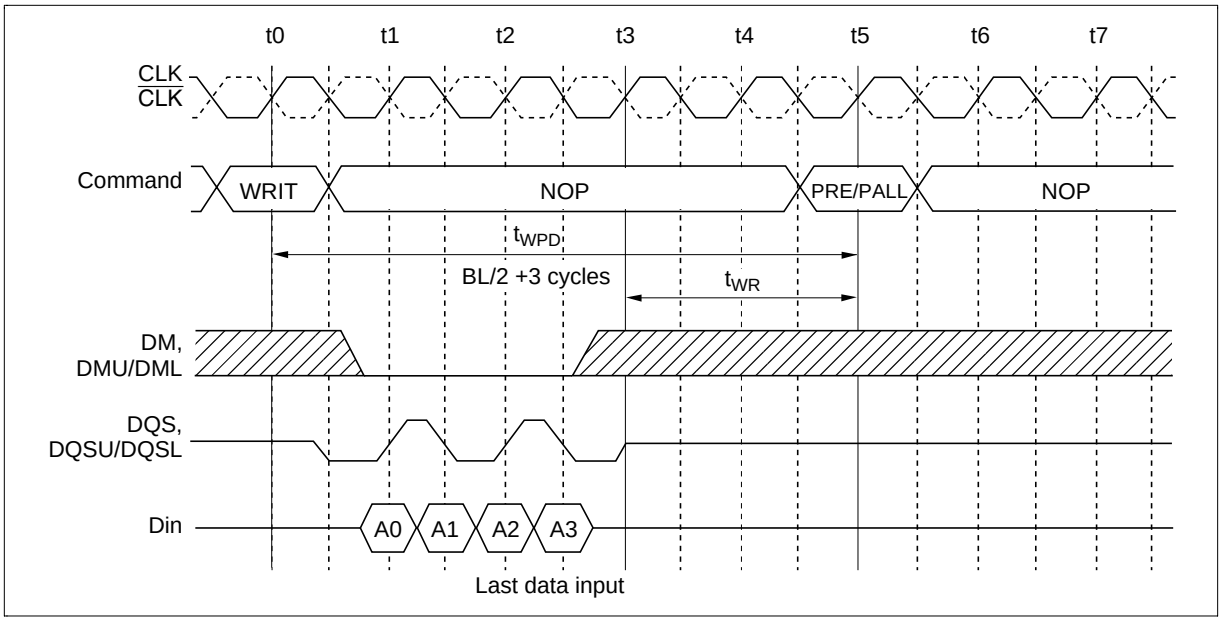
$\overline{CAS}$ Latency = 2.5, Burst Length = 2, 4, 8



A Write command to the consecutive Precharge command interval (same bank): The minimum interval t_{WPD} ((BL/ 2 + 3) cycles) is necessary between the write command and the precharge command.

WRITE to PRECHARGE Command Interval (same bank)

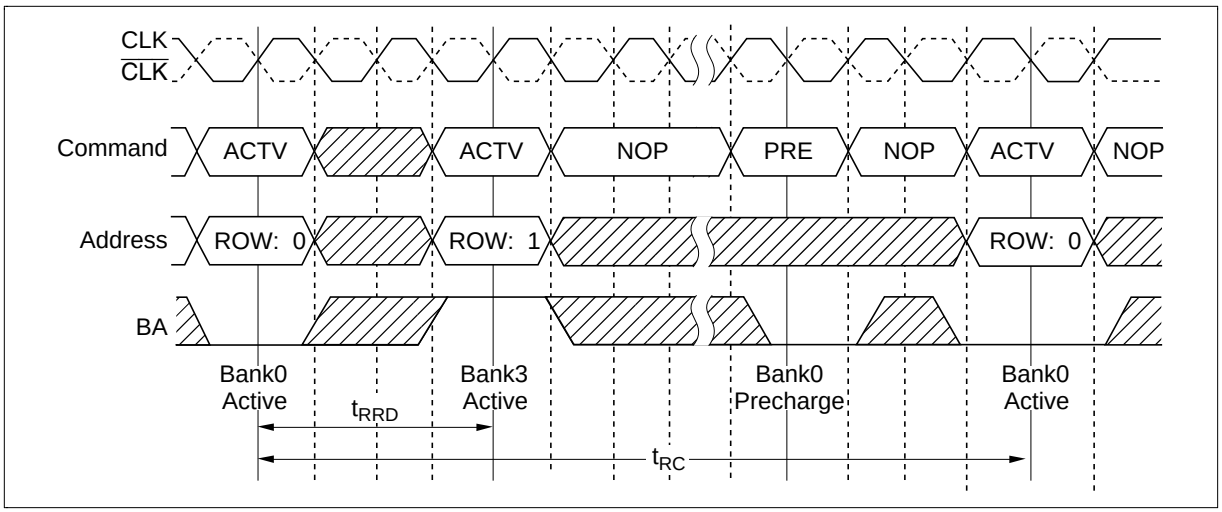
Burst Length = 4



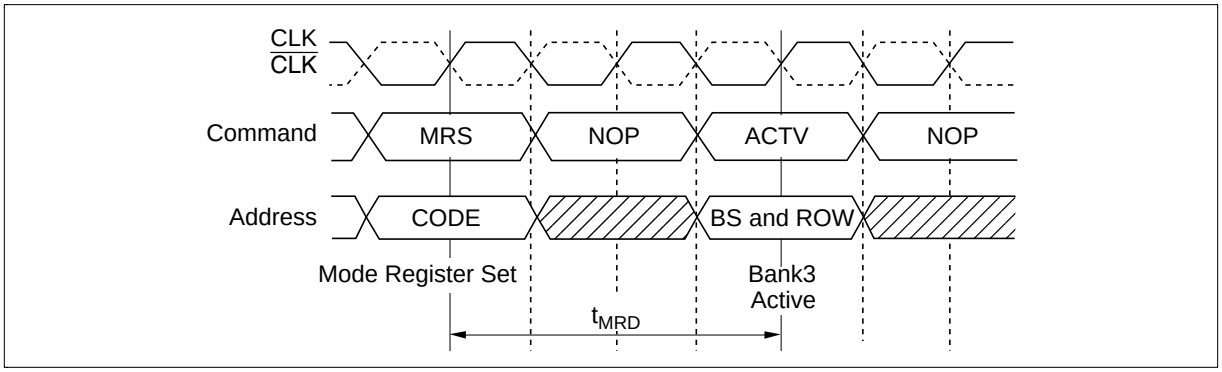
Bank active command interval:

	Destination row of the consecutive ACTV command			
	Bank address	**Row address**	**State**	**Operation**
1.	Same	Any	ACTIVE	Two successive ACTV commands can be issued at t_{RC} interval. In between two successive ACTV operations, precharge command should be executed.
2.	Different	Any	ACTIVE	Prechage the bank. t_{RP} after the precharge command, the consecutive ACTV command can be issued.
			IDLE	t_{RRD} after an ACTV command, the next ACTV command can be issued.

Bank Active to Bank Active



Mode register set to Bank-active command interval: The interval between setting the mode register and executing a bank-active command must be no less than t_{MRD}.

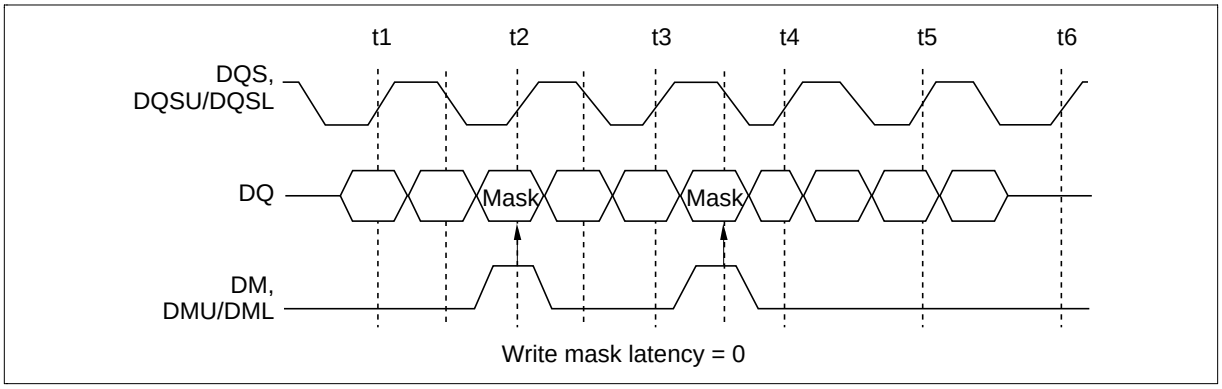


DMU/DML Control (HM5425161B)

DMU can mask upper byte of input data. DML can mask lower byte of input data. By setting DMU/DML to Low, data can be written. When DMU/DML is set to High, the corresponding data is not written, and the previous data is held. The latency between DMU/DML input and enabling/disabling mask function is 0.

DM Control (HM5425801B/HM5425401B)

DM can mask input data. By setting DM to Low, data can be written. When DM is set to High, the corresponding data is not written, and the previous data is held. The latency between DM input and enabling/disabling mask function is 0.



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to V_{ss}	V_T	–1.0 to +4.6	V	1
Supply voltage relative to V_{SS}	V_{CC}, V_{CCQ}	–1.0 to +4.6	V	1
Short circuit output current	Iout	50	mA	
Power dissipation	P_T	1.0	W	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	–55 to +125	°C	

Note: 1. Refer to V_{SS}.

DC Operating Conditions (Ta = 0 to +70˚C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}, V_{CCQ}	2.3	2.5	2.7	V	1, 2
	V_{SS}, V_{SSQ}	0	0	0	V	
Input reference voltage	V_{REF}	1.15	1.25	1.35	V	1
Termination voltage	V_{TT}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V	1
DC Input high voltage	V_{IH}	V_{REF} + 0.18	—	V_{CCQ} + 0.3	V	1, 3
DC Input low voltage	V_{IL}	–0.3	—	V_{REF} – 0.18	V	1, 4
DC Input signal voltage	V_{IN} (dc)	–0.3	—	V_{CCQ} + 0.3	V	5
DC differential input voltage	V_{SWING} (dc)	0.36	—	V_{CCQ} + 0.6	V	6

Notes: 1. All parameters are referred to V_{SS}, when measured.
2. V_{CCQ} must be lower than or equal to V_{CC}.
3. V_{IH} is allowed to exceed V_{CC} up to 4.6 V for the period shorter than or equal to 5 ns.
4. V_{IL} is allowed to outreach below V_{SS} down to –1.0 V for the period shorter than or equal to 5 ns.
5. V_{IN} (dc) specifies the allowable dc execution of each differential input.
6. V_{SWING} (dc) specifies the input differential voltage required for switching.

DC Characteristics (Ta = 0 to +70˚C, V_{CC}, V_{CCQ} = 2.5 V ± 0.2 V, V_{SS}, V_{SSQ} = 0 V) (HM5425161B)

		HM5425161B								
		-75A		-75B		-10				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions	Notes
Operating current (ACTV-PRE)	I_{CC0}	—	TBD	—	TBD	—	TBD	mA	CKE ≥ V_{IH}, t_{RC} = min	1, 2, 5
Operating current (ACTV-READ-PRE)	I_{CC1}	—	TBD	—	TBD	—	TBD	mA	CKE ≥ V_{IH}, BL = 2, CL = 2.5, t_{RC} = min	1, 2, 5
Idle power down standby current	I_{CC2P}	—	TBD	—	TBD	—	TBD	mA	CKE ≤ V_{IL}	4
Idle standby current	I_{CC2N}	—	TBD	—	TBD	—	TBD	mA	CKE ≥ V_{IH}, $\overline{CS}$ ≥ V_{IH}	4
Active power down standby current	I_{CC3P}	—	TBD	—	TBD	—	TBD	mA	CKE ≤ V_{IL}	3
Active standby current	I_{CC3N}	—	TBD	—	TBD	—	TBD	mA	CKE ≥ V_{IH}, t_{RAS} = max	3
Operating current (Burst read operation)	I_{CC4R}	—	TBD	—	TBD	—	TBD	mA	CKE ≥ V_{IH}, BL = 2, CL = 2.5	1, 2, 5, 6
Operating current (Burst write operation)	I_{CC4W}	—	TBD	—	TBD	—	TBD	mA	CKE ≥ V_{IH}, BL = 2, CL = 2.5	1, 2, 5, 6
Auto refresh current	I_{CC5}	—	TBD	—	TBD	—	TBD	mA	t_{RFC} = min, Input ≤ V_{IL} or ≥ V_{IH}	
Self refresh current	I_{CC6}	—	2	—	2	—	2	mA	Input ≥ V_{CC} – 0.2 V Input ≤ 0.2 V	
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	V_{CC} ≥ Vin ≥ V_{SS}	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	V_{CC} ≥ Vout ≥ V_{SS}	
Output high voltage	V_{OH}	V_{TT} + 0.76	—	V_{TT} + 0.76	—	V_{TT} + 0.76	—	V	I_{OH} (max) = –15.2 mA	
Output low voltage	V_{OL}	—	V_{TT} – 0.76	—	V_{TT} – 0.76	—	V_{TT} – 0.76	V	I_{OL} (min) = 15.2 mA	

Notes. 1. These I_{CC} data are measured under condition that DQ pins are not connected.
2. One bank operation.
3. One bank active.
4. All banks idle.
5. Command/Address transition once per one cycle.
6. Data/Data mask transition twice per one cycle.
7. The I_{CC} data on this table are measured with regard to t_{CK} = min in general.

DC Characteristics (Ta = 0 to +70˚C, V_{CC}, V_{CCQ} = 2.5 V ± 0.2 V, V_{SS}, V_{SSQ} = 0 V) (HM5425801B/HM5425401B)

		HM5425801B/HM5425401B								
		-75A		-75B		-10				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current (ACTV-PRE)	I_{CC0}	—	TBD	—	TBD	—	TBD	mA	CKE ≥ V_{IH}, t_{RC} = min	1, 2, 5
Operating current (ACTV-READ-PRE)	I_{CC1}	—	TBD	—	TBD	—	TBD	mA	CKE ≥ V_{IH}, BL = 2, CL = 2.5, t_{RC} = min	1, 2, 5
Idle power down standby current	I_{CC2P}	—	TBD	—	TBD	—	TBD	mA	CKE ≤ V_{IL}	4
Idle standby current	I_{CC2N}	—	TBD	—	TBD	—	TBD	mA	CKE ≥ V_{IH}, $\overline{CS}$ ≥ V_{IH}	4
Active power down standby current	I_{CC3P}	—	TBD	—	TBD	—	TBD	mA	CKE ≤ V_{IL}	3
Active standby current	I_{CC3N}	—	TBD	—	TBD	—	TBD	mA	CKE ≥ V_{IH}, t_{RAS} = max	3
Operating current (Burst read operation)	I_{CC4R}	—	TBD	—	TBD	—	TBD	mA	CKE ≥ V_{IH}, BL = 2, CL = 2.5	1, 2, 5, 6
Operating current (Burst write operation)	I_{CC4W}	—	TBD	—	TBD	—	TBD	mA	CKE ≥ V_{IH}, BL = 2, CL = 2.5	1, 2, 5, 6
Auto Refresh current	I_{CC5}	—	TBD	—	TBD	—	TBD	mA	t_{RFC} = min, Input ≤ V_{IL} or ≥ V_{IH}	
Self refresh current	I_{CC6}	—	2	—	2	—	2	mA	Input ≥ V_{CC} – 0.2 V Input ≤ 0.2 V	
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	V_{CC} ≥ Vin ≥ V_{SS}	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	V_{CC} ≥ Vout ≥ V_{SS}	
Output high voltage	V_{OH}	V_{TT} + 0.76	—	V_{TT} + 0.76	—	V_{TT} + 0.76	—	V	I_{OH} (max) = –15.2 mA	
Output low voltage	V_{OL}	—	V_{TT} – 0.76	—	V_{TT} – 0.76	—	V_{TT} – 0.76	V	I_{OL} (min) = 15.2 mA	

Notes: 1. These I_{CC} data are measured under condition that DQ pins are not connected.
2. One bank operation.
3. One bank active.
4. All banks idle.
5. Command/Address transition once per one clock cycle.
6. Data/Data mask transition twice per one clock cycle.
7. The I_{CC} data on this table are measured with regard to t_{CK} = min in general.

Capacitance (Ta = 25°C, V_{CC}, V_{CCQ} = 2.5 V ± 0.2 V)

Parameter	Symbol	Min	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	2.5	3.5	pF	1
Input capacitance (Command)	C_{I2}	2.5	3.5	pF	1
Data and DOS input/output capacitance (I/O)	C_O	4	5.5	pF	1, 2

Notes: 1. These parameters are measured on conditions: f = 100 MHz, Vout = V_{CCQ}/2, ΔVout = 0.2 V.
2. Dout circuits are disabled.

AC Characteristics (Ta = 0 to +70˚C, V_{CC}, V_{CCQ} = 2.5 V ± 0.2 V, V_{SS}, V_{SSQ} = 0 V)

		HM5425161B/HM542581B/HM5425401B							
		-75A		-75B		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Clock cycle time ($\overline{CAS}$ latency = 2)	t_{CK}	7.5	15	10	15	10	15	ns	10
($\overline{CAS}$ latency = 2.5)	t_{CK}	7	15	7.5	15	8	15	ns	
Input clock high level time	t_{CH}	0.45	—	0.45	—	0.45	—	t_{CK}	
Input clock low level time	t_{CL}	0.45	—	0.45	—	0.45	—	t_{CK}	
CLK to DQS skew	t_{DQSCK}	–0.7	0.7	–0.7	0.7	–0.8	0.8	ns	2
DATA to CLK skew	t_{AC}	–0.7	0.7	–0.7	0.7	–0.8	0.8	ns	2
Dout to DQS skew	t_{DQSQ}	–0.5	0.5	–0.5	0.5	–0.6	0.6	ns	3
Dout/DQS valid window	t_{DV}	0.35	—	0.35	—	0.35	—	t_{CK}	4
DQS valid window	t_{DQSV}	0.35	—	0.35	—	0.35	—	t_{CK}	4
DQS read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	
DQS read postamble	t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	
Dout-High impedance delay from CLK/$\overline{CLK}$	t_{HZ}	–0.7	0.7	–0.7	0.7	–0.8	0.8	ns	5
Dout-Low impedance delay from CLK/$\overline{CLK}$	t_{LZ}	–0.7	0.7	–0.7	0.7	–0.8	0.8	ns	6
DQ and DM input pulse width	t_{DIPW}	1.7	—	1.7	—	2	—	ns	7
Data and data mask to data strobe setup time	t_{DS}	0.5	—	0.5	—	0.6	—	ns	8
Data and data mask to data strobe hold time	t_{DH}	0.5	—	0.5	—	0.6	—	ns	8
Clock to DQS write preamble setup time	t_{WPRES}	0	—	0	—	0	—	ns	
Clock to DQS write preamble hold time	t_{WPREH}	0.25	—	0.25	—	0.25	—	t_{CK}	
DQS last edge to High-Z time (DQS write postamble)	t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	9
Clock to the DQS first rising edge for write delay	t_{DQSS}	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	

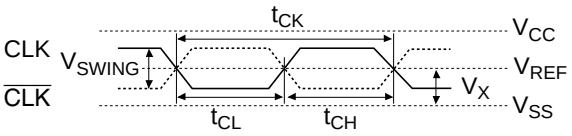
		HM5425161B/HM5425801B/HM5425401B							
		-75A		-75B		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
DQS falling edge to CLK setup time	t_{DSS}	0.2	—	0.2	—	0.2	—	t_{CK}	
DQS falling edge hold time to CLK	t_{DSH}	0.2	—	0.2	—	0.2	—	t_{CK}	
DQS high pulse width (DQS write)	t_{DQSH}	0.35	—	0.35	—	0.35	—	t_{CK}	
DQS low pulse width (DQS write)	t_{DQSL}	0.35	—	0.35	—	0.35	—	t_{CK}	
Input command and address setup time	t_{IS}	1.1	—	1.1	—	1.2	—	ns	8
Input command and address hold time	t_{IH}	1.1	—	1.1	—	1.2	—	ns	8
Active command period	t_{RC}	65	—	65	—	70	—	ns	
Auto refresh to active/Auto refresh command cycle	t_{RFC}	75	—	75	—	80	—	ns	
Active to Precharge command period	t_{RAS}	45	120000	45	120000	50	120000	ns	
Active to column command period	t_{RCD}	20	—	20	—	20	—	ns	
Last data in to precharge	t_{WR}	15	—	15	—	15	—	ns	
Precharge to active command period	t_{RP}	20	—	20	—	20	—	ns	
Active to active command period	t_{RRD}	15	—	15	—	15	—	ns	
Average periodic refresh interval	t_{REF}	—	7.8	—	7.8	—	7.8	µs	

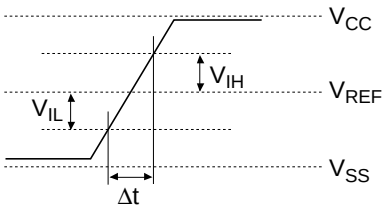
Notes. 1. On all AC measurements, we assume the test conditions shown in the next page. For timing parameter definitions, see 'Timing Waveforms' section.

2. This parameter defines the signal transition delay from the cross point of CLK and $\overline{CLK}$. The signal transition is defined to occur when the signal level crossing V_{TT}.
3. The timing reference level is V_{TT}.
4. Output valid window is defined to be the period between two successive transition of data out or DQS (read) signals. The signal transition is defined to occur when the signal level crossing V_{TT}.
5. t_{HZ} is defined as Dout transition delay from Low-Z to High-Z at the end of read burst operation. The timing reference is cross point of CLK and $\overline{CLK}$. This parameter is not referred to a specific Dout voltage level, but specify when the device output stops driving.
6. t_{LZ} is defined as Dout transition delay from High-Z to Low-Z at the beginning of read operation. This parameter is not referred to a specific Dout voltage level, but specify when the device output begins driving.
7. Input valid windows is defined to be the period between two successive transition of data input or DQS (write) signals. The signal transition is defined to occur when the signal level crossing V_{REF}.
8. The timing reference level is V_{REF}.
9. The transition from Low-Z to High-Z is defined to occur when the device output stops driving. A specific reference voltage to judge this transition is not given.
10. t_{CK} max is determined by the lock range of the DLL. Beyond this lock range, the DLL operation is not assured.
11. V_{CC} is assumed to be 2.5 V ± 0.2 V. V_{CC} power supply variation per cycle expected to be less than 0.4 V/400 cycle.

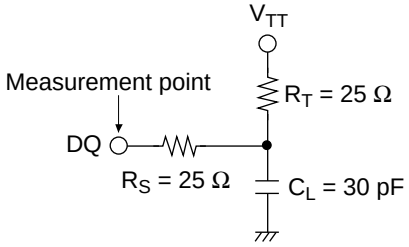
Test Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input reference voltage	V_{REF}	1.15	1.25	1.35	V
Termination voltage	V_{TT}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
AC input high voltage	V_{IH} (ac)	V_{REF} + 0.35	—	—	V
AC input low voltage	V_{IL} (ac)	—	—	V_{REF} – 0.35	V
AC differential input high voltage	V_{SWING} (ac)	0.7	—	V_{CCQ} + 0.6	V
AC differential cross point voltage	V_X (ac)	V_{REF} – 0.2	V_{REF}	V_{REF} + 0.2	V
Input signal slew rate	SLEW	—	1	—	V/ns





SLEW = (V_{IH} (ac) – V_{IL} (ac))/Δt

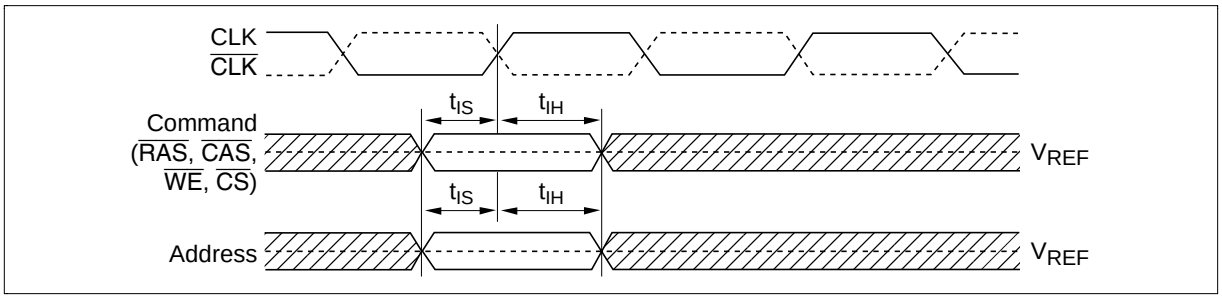


Timing Parameter Measured in Clock Cycle

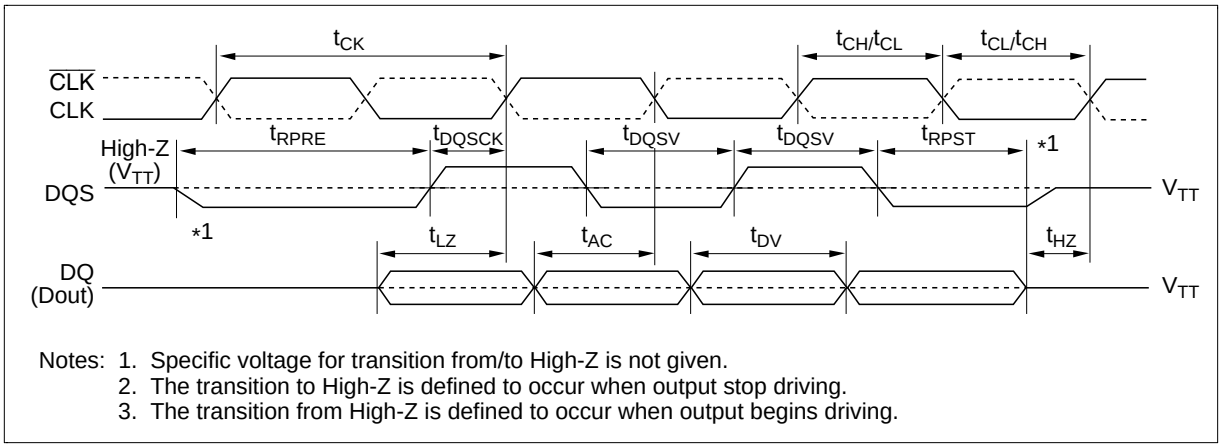
Parameter	Symbol	Number of clock cycle	
		Min	Max
Write to pre-charge command delay (same bank)	t_{WPD}	3 + BL/2	
Read to pre-charge command delay (same bank)	t_{RPD}	BL/2	
Write to read command delay (to input all data)	t_{WRD}	2 + BL/2	
Burst stop command to write command delay ($\overline{CAS}$ latency = 2)	t_{BSTW}	2	
($\overline{CAS}$ latency = 2.5)	t_{BSTW}	3	
Burst stop command to DQ High-Z ($\overline{CAS}$ latency = 2)	t_{BSTZ}	2	
($\overline{CAS}$ latency = 2.5)	t_{BSTZ}	2.5	
Read command to write command delay (to output all data) ($\overline{CAS}$ latency = 2)	t_{RWD}	2 + BL/2	
($\overline{CAS}$ latency = 2.5)	t_{RWD}	3 + BL/2	
Pre-charge command to High-Z ($\overline{CAS}$ latency = 2)	t_{HZP}	2	
($\overline{CAS}$ latency = 2.5)	t_{HZP}	2.5	
Write command to data in latency	t_{WCD}	1	
Write recovery	t_{WR}	2	
DM to data in latency	t_{DMD}	0	
Register set command to active or register set command	t_{MRD}	2	
Self refresh exit to non-read command	t_{SNR}	10	
Self refresh exit to read command	t_{SRD}	200	
Power down entry	t_{PDEN}		1
Power down exit to command input	t_{PDEX}		1
CKE minimum pulse width	t_{CKEPW}	1	

Timing Waveforms

Command and Addresses Input Timing Definition

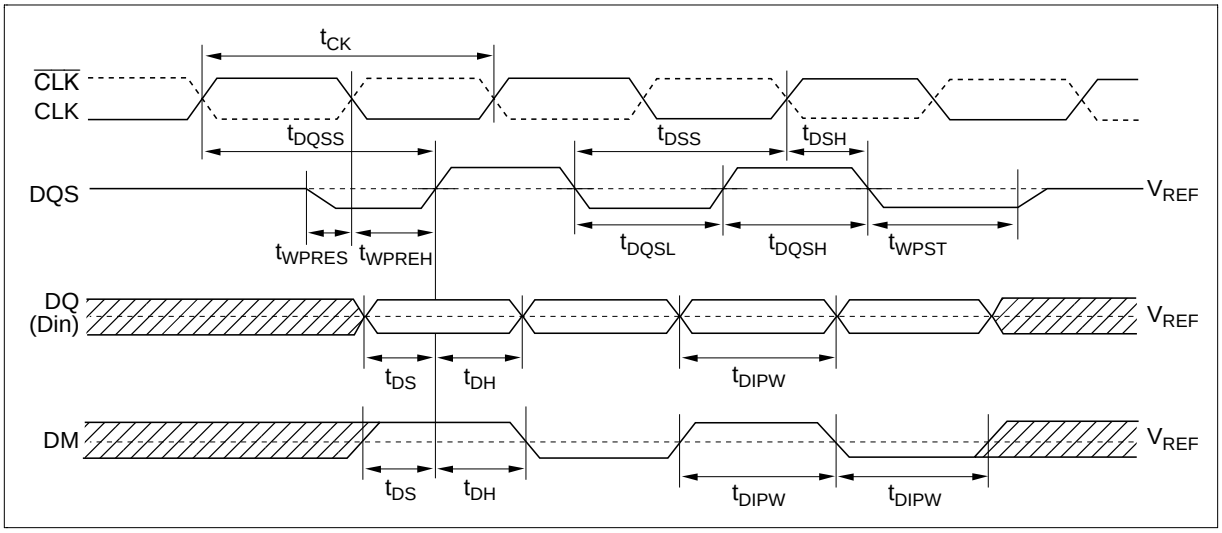


Read Timing Definition

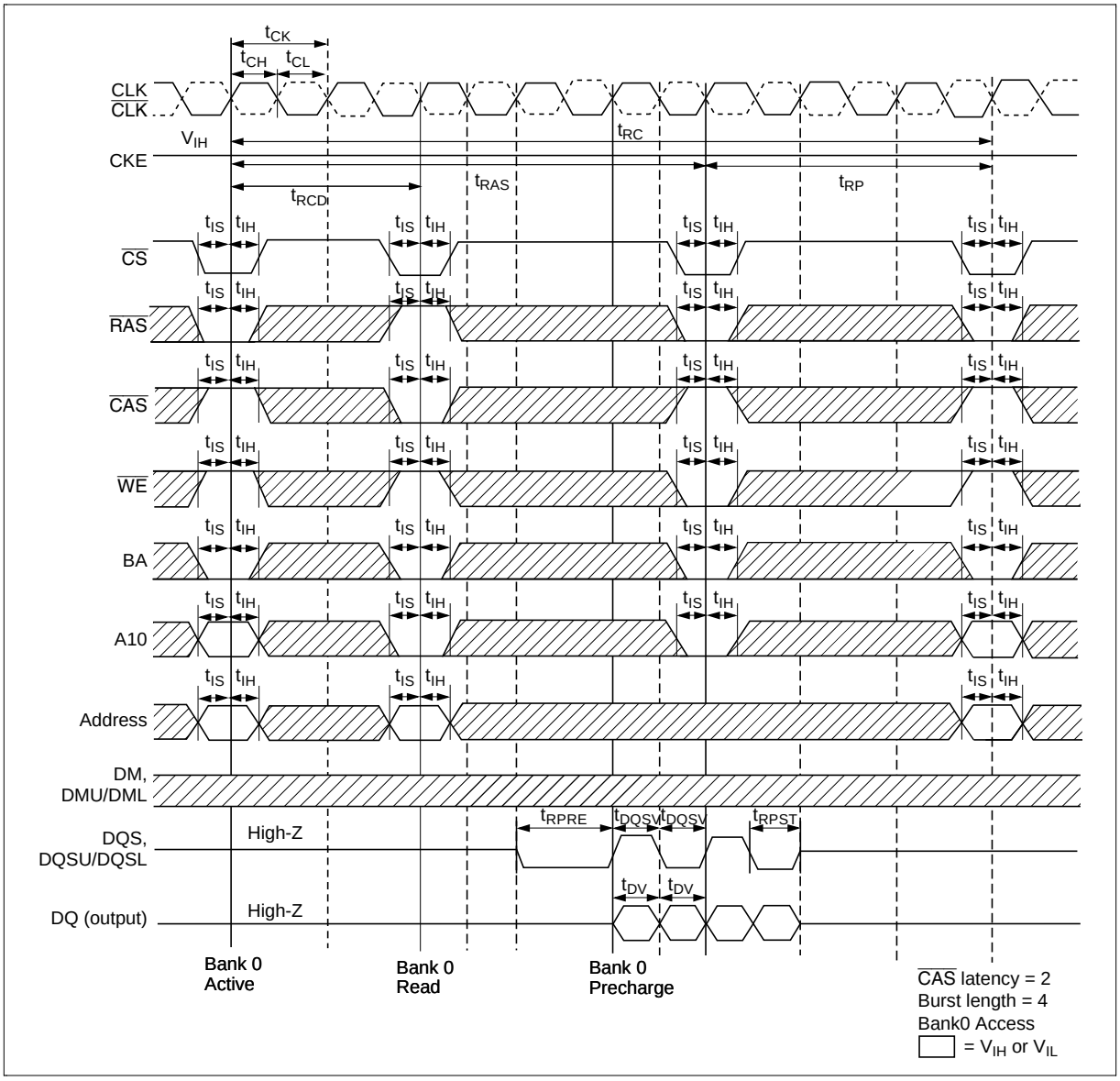


Notes: 1. Specific voltage for transition from/to High-Z is not given.
2. The transition to High-Z is defined to occur when output stop driving.
3. The transition from High-Z is defined to occur when output begins driving.

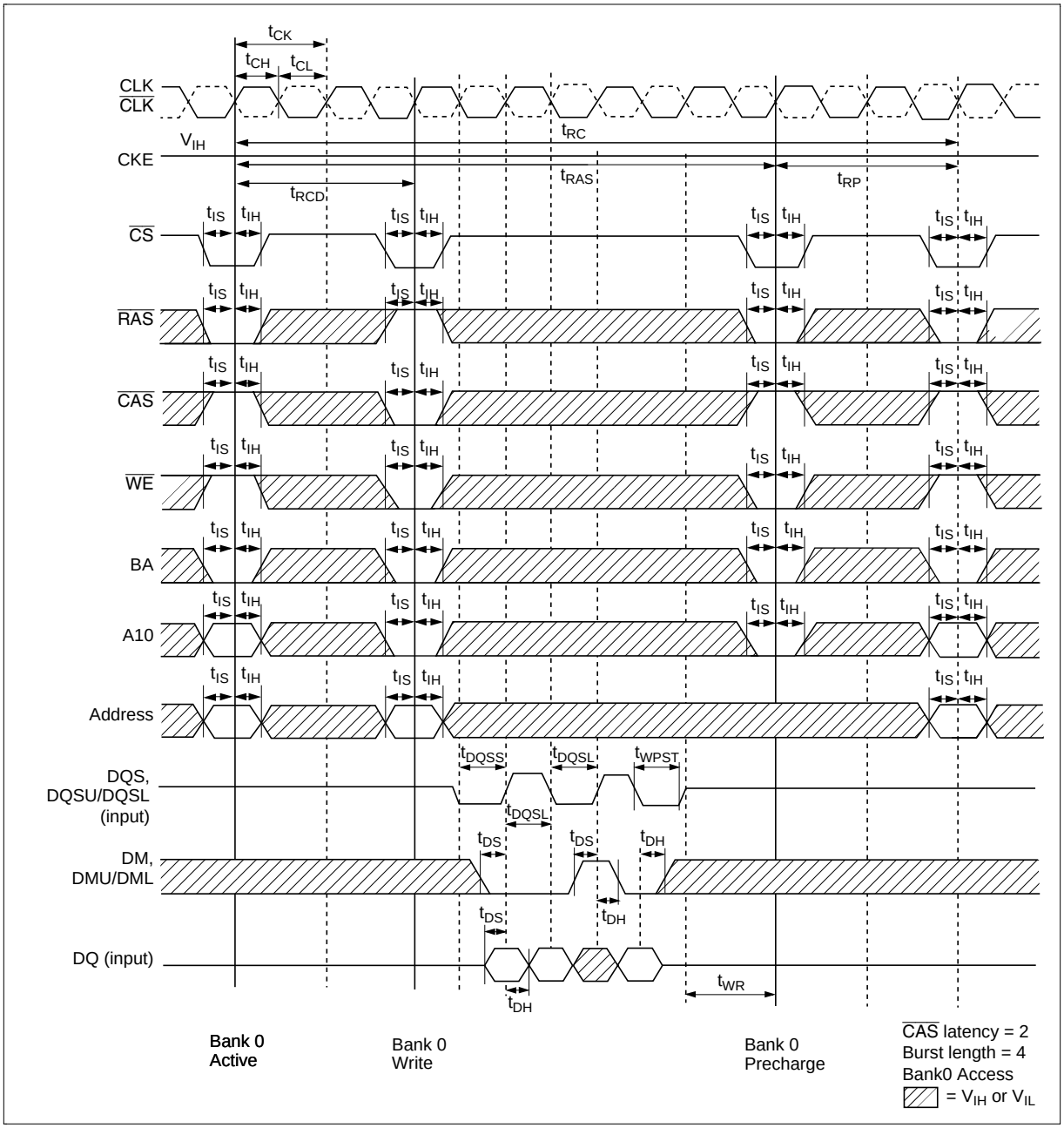
Write Timing Definition



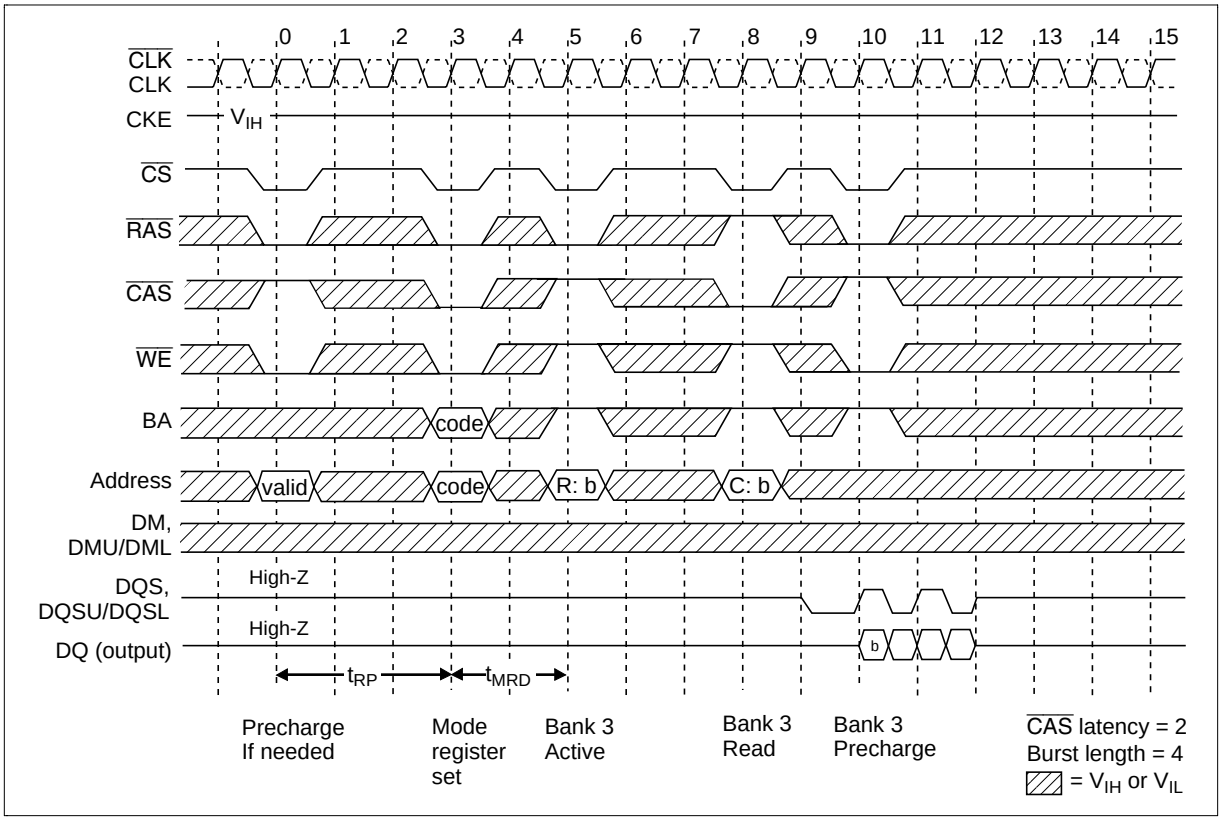
Read Cycle


tCK
tCH
tCL
CLK
CLK
VIH
CKE
tRC
tRAS
tRP
tRCD
tIS
tIH
CS
RAS
CAS
WE
BA
A10
Address
DM,
DMU/DML
DQS,
DQSU/DQSL
DQ (output)
High-Z
tRPRE
tDQSV
tRPST
tDV
Bank 0
Active
Bank 0
Read
Bank 0
Precharge
CAS latency = 2
Burst length = 4
Bank0 Access
= VIH or VIL

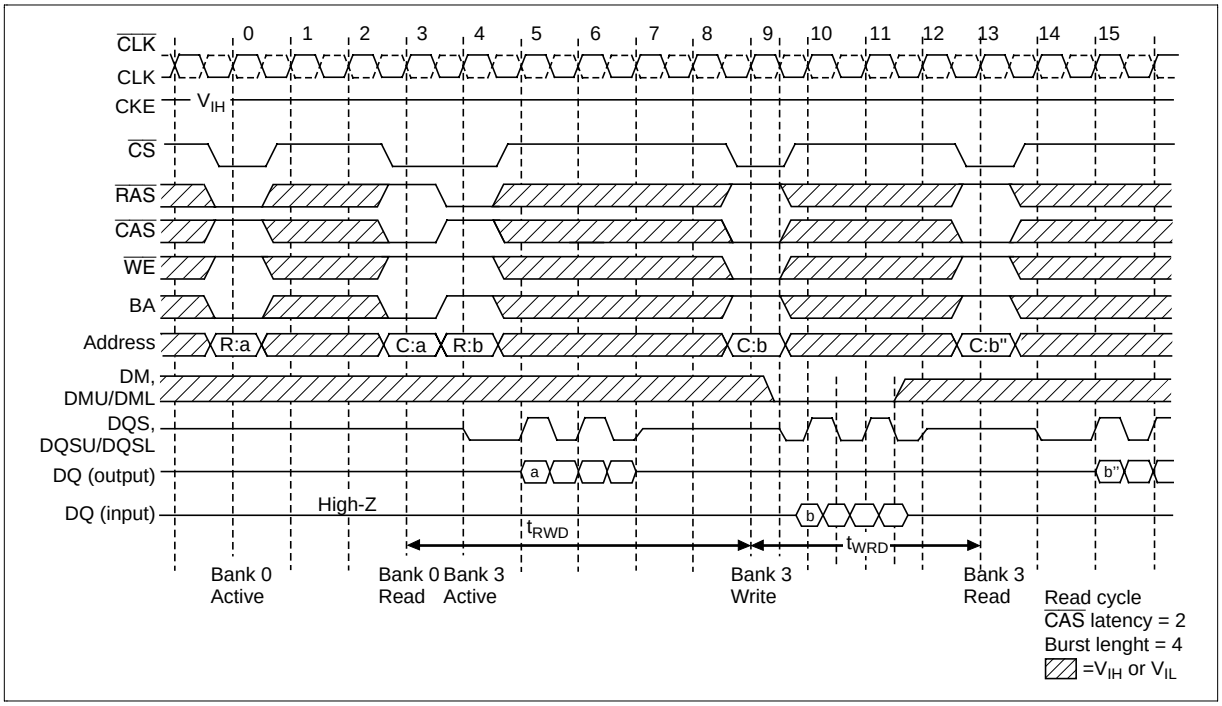
Write Cycle


tCK
tCH
tCL
CLK
CLK
VIH
CKE
tRC
tRAS
tRP
tRCD
CS
RAS
CAS
WE
BA
A10
Address
tIS
tIH
tDQSS
tDQSL
tWPST
DQS,
DQSU/DQSL
(input)
tDS
tDH
DM,
DMU/DML
DQ (input)
tWR
Bank 0
Active
Bank 0
Write
Bank 0
Precharge
CAS latency = 2
Burst length = 4
Bank0 Access
= VIH or VIL

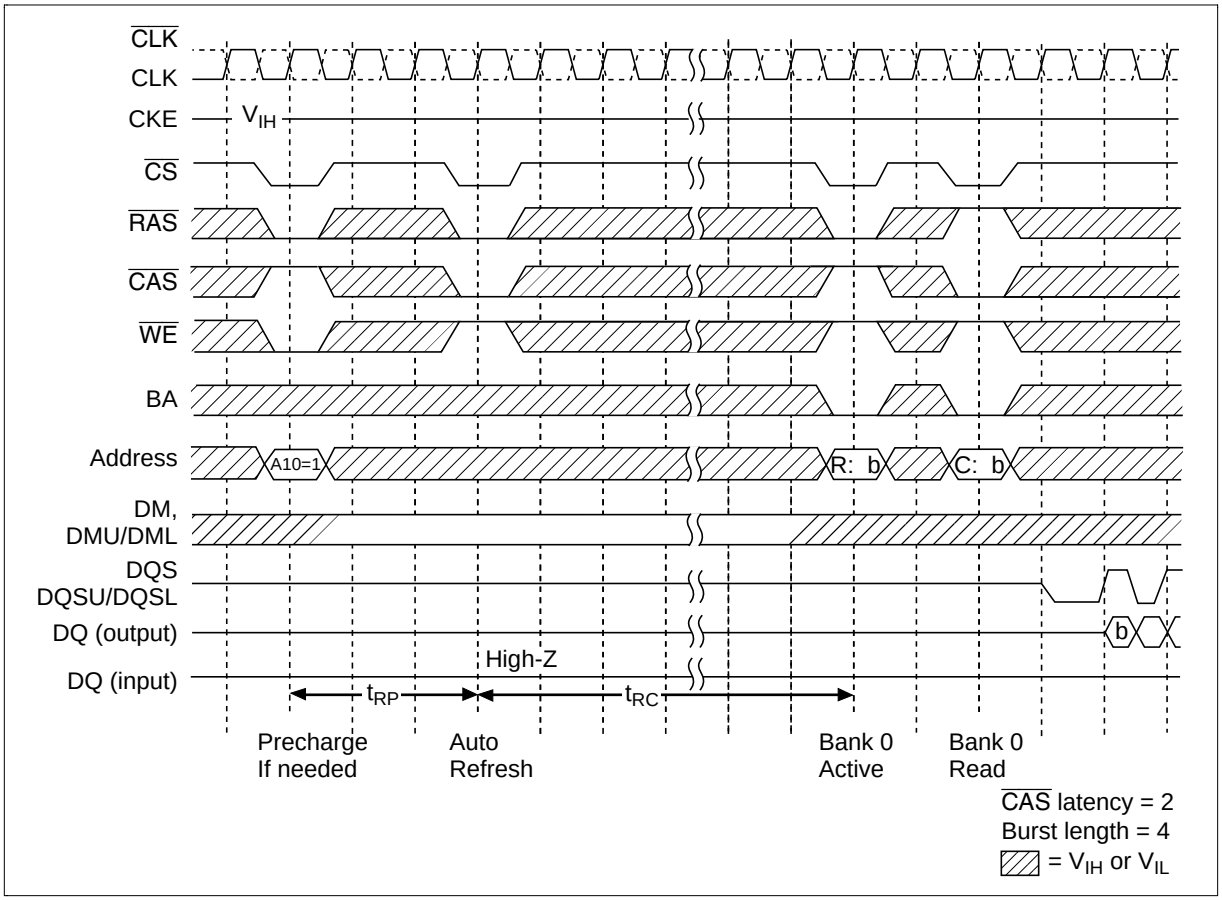
Mode Register Set Cycle



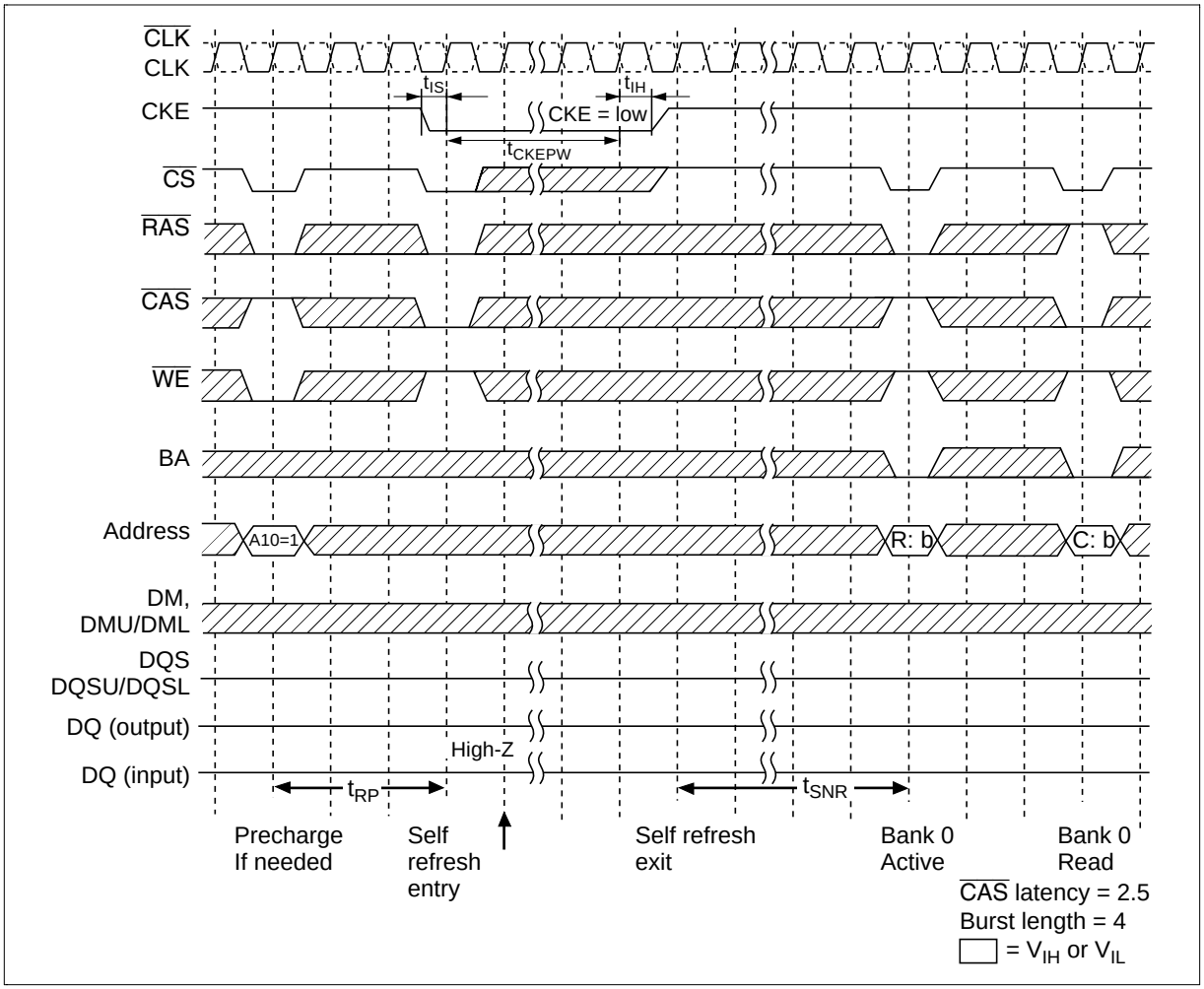
Read/Write Cycle



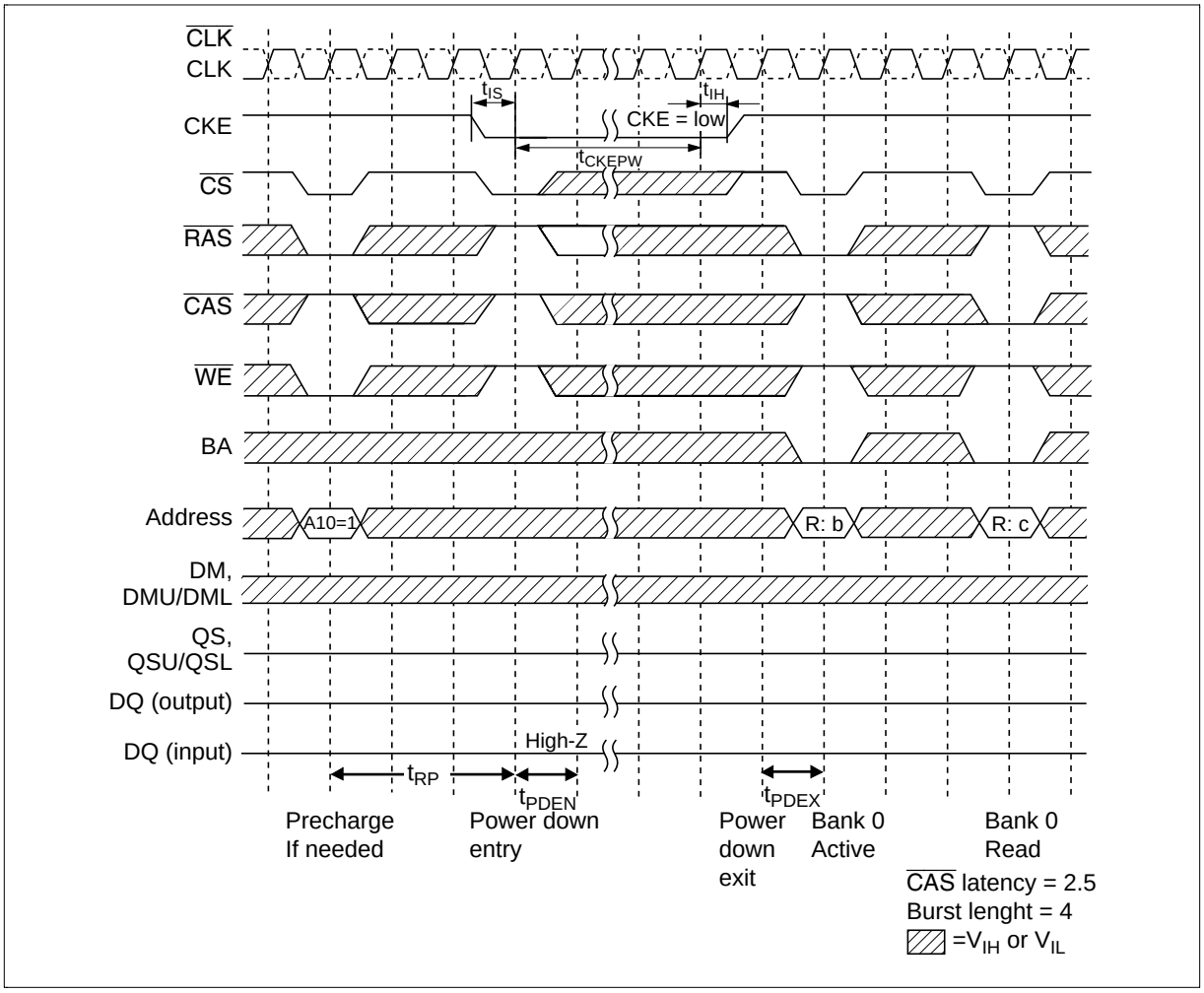
Auto Refresh Cycle



Self Refresh Cycle



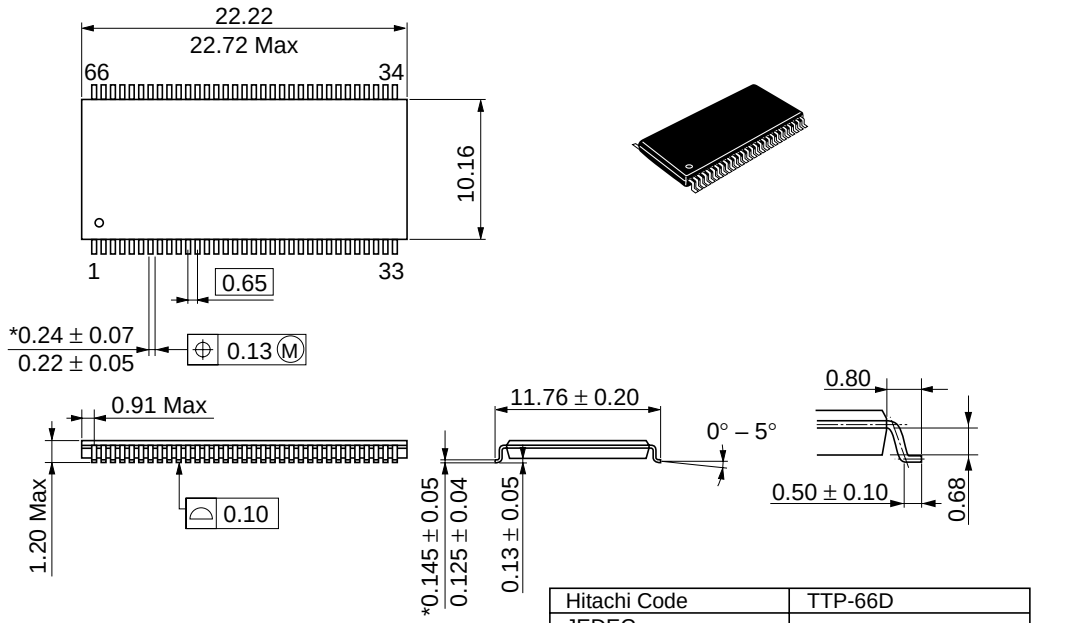
Power Down Mode



Package Dimensions

HM5425161BTT/HM5425801BTT/HM5425401BTT Series (TTP-66D)

Preliminary Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-66D
JEDEC	—
EIAJ	—
Weight (reference value)	0.53 g

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