ST7 FAMILY

8-BIT MCUs

PRODUCT OVERVIEW

JULY 1998

USE IN LIFE SUPPORT DEVICES OR SYSTEMS MUST BE EXPRESSLY AUTHORIZED.

STMicroelectronics PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF STMicroelectronics. As used herein:

1. Life support devices or systems are those which (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided with the product, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can reasonably be expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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ST7 PRODUCT FINDER

	Device	OTP/ EPROM/ ROM x 8	RAM x 8	EEPROM x8	8-bit ADC Inputs	Watch-dog	16-bit Timers	Serial Comm. (Sync)	Serial Comm. (Async)	I/Os (High Current)	Package	Additional Features
BASIC	**ST72101G1**	4K	256	-	-	Yes	1	SPI	-	22 (8)	SDIP32/ SO28	
	ST72101G2	8K	256	-	-	Yes	1	SPI	-	22 (8)	SDIP32/ SO28	
	ST72121J2	8K	384	-	-	Yes	2	SPI	SCI	32 (4)	SDIP42/ TQFP44	Low Voltage Detector
	ST72121J4	16K	512	-	-	Yes	2	SPI	SCI	32 (4)	SDIP42/ TQFP44	
ADC	**ST72213G1**	4K	256	-	6	Yes	1	SPI	-	22 (8)	SDIP32/ SO28	
	ST72212G2	8K	256	-	6	Yes	2	SPI	-	22 (8)	SDIP32/ SO28	
	ST72311J2	8K	384	-	6	Yes	2	SPI	SCI	32 (4)	SDIP42/ TQFP44	Low Voltage Detector
	ST72311J4	16K	512	-	6	Yes	2	SPI	SCI	32 (4)	SDIP42/ TQFP44	
	ST72311N2	8K	384	-	8	Yes	2	SPI	SCI	44 (8)	SDIP56/ TQFP64	
	ST72311N4	16K	512	-	8	Yes	2	SPI	SCI	44 (8)	SDIP56/ TQFP64	
	ST72311N6*	32K	1024	-	8	Yes	2	SPI	SCI	44 (8)	TQFP64	
ADC+EEPROM	**ST72331J2**	8K	384	256	6	Yes	2	SPI	SCI	32 (4)	SDIP42/ TQFP44	Low Voltage Detector
	ST72331J4	16K	512	256	6	Yes	2	SPI	SCI	32 (4)	SDIP42/ TQFP44	
	ST72331N2	8K	384	256	8	Yes	2	SPI	SCI	44 (8)	SDIP56/ TQFP64	
	ST72331N4	16K	512	256	8	Yes	2	SPI	SCI	44 (8)	SDIP56/ TQFP64	
	ST72331N6*	32K	1024	256	8	Yes	2	SPI	SCI	44 (8)	TQFP64	
ADC+PWM	**ST72272K2**	8K	384	-	4	Yes	1	-	-	24 (4)	SDIP32/ SO34	DAC with PWM outputs
	ST72272K4	16K	512	-	4	Yes	1	-	-	24 (4)	SDIP32/ SO34	
	ST72372J4	16K	512	-	4	Yes	1	I^2C	-	30 (6)	SDIP42/ TQFP44	
	ST72371N4	16K	512	-	8	Yes	1	I^2C	SCI	39 (8)	SDIP56/ TQFP64	
I^2C	**ST72251G1**	4K	256	-	6	Yes	2	I^2C+SPI	-	22 (8)	SDIP32/ SO28	
	ST72251G2	8K	256	-	6	Yes	2	I^2C+SPI	-	22 (8)	SDIP32/ SO28	

	Device	OTP/ EPROM/ ROM x 8	RAM x 8	EEPROM x8	8-bit ADC Inputs	Watch-dog	16-bit Timers	Serial Comm. (Sync)	Serial Comm. (Async)	I/Os (High Current)	Package	Additional Features
CAN	**ST72512N2***	8K	384	-	8	Yes	1	SPI	-	44 (4)	SDIP56/ TQFP64	CAN peripheral
	ST72511R4*	16K	512	-	8	Yes	2	SPI	SCI	44 (4)	TQFP64	
	ST72511R6*	32K	1024	-	8	Yes	2	SPI	SCI	44 (4)	TQFP64	
	ST72532N2*	8K	384	256	8	Yes	1	SPI	-	44 (4)	SDIP56/ TQFP64	
	ST72531R4*	16K	512	256	8	Yes	2	SPI	SCI	44 (4)	TQFP64	
	ST72531R6*	32K	1024	256	8	Yes	2	SPI	SCI	44 (4)	TQFP64	
USB	**ST72671N4***	16K	512	-	8	Yes	1	I^2C	SCI	34 (8)	SDIP56/ TQFP64	USB peripheral + DAC with PWM outputs
	ST72671N6*	32K	1024	-	8	Yes	1	I^2C	SCI	34 (8)	SDIP56/ TQFP64	

* Not yet available. Contact sales office for data and availability.

Abbreviations:

ADC = Analog to Digital Converter
CAN = Controller Area Network
DAC = Digital to Analog Converter
I^2C = I^2C Multimaster
PWM = Pulse Width Modulation
SCI = Serial Communications Interface
SPI = Serial Peripheral Interface
USB = Universal Serial Bus
WDG = Watchdog

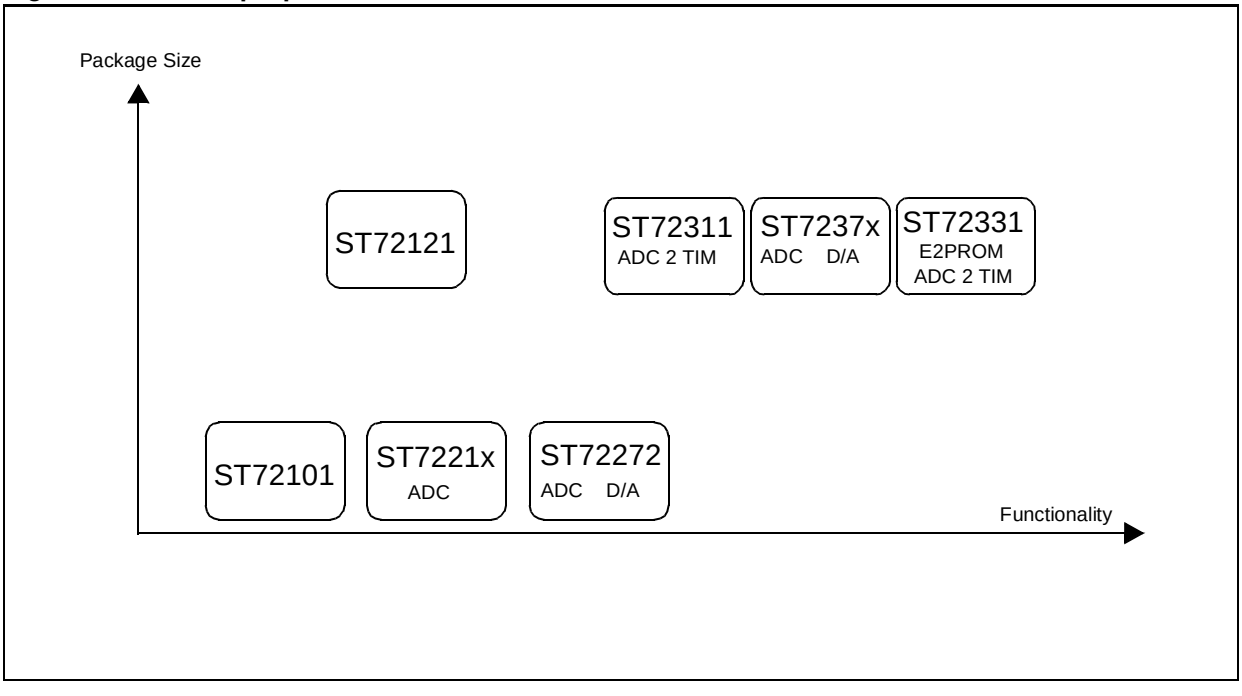
Packages:

DIP = Dual In Line
SO = Small Outline
QFP = Quad Flat Pack
S = Shrink
T = Thin

INTRODUCTION

The ST7 Industry-Standard microcontroller family offers a wide range of MCU solutions for industrial, automotive (CAN), computer peripherals (USB) and consumer applications. The ST7 has been used for many years in high volume dedicated applications such as monitors and car radios. Based on an industry-standard 8-bit architecture, extended by STMicroelectronics to better accommodate high level language programming, the ST7 is designed to target small and medium sized applications with the requirements of excellent system price/performance, short application development cycle and outstanding quality and reliability. The powerful on-chip peripherals add functionality to the ST7 core and a range of different versions and package sizes to allow the user select the device that best matches the needs of the application.

Figure 1. ST7 Multipurpose Microcontrollers



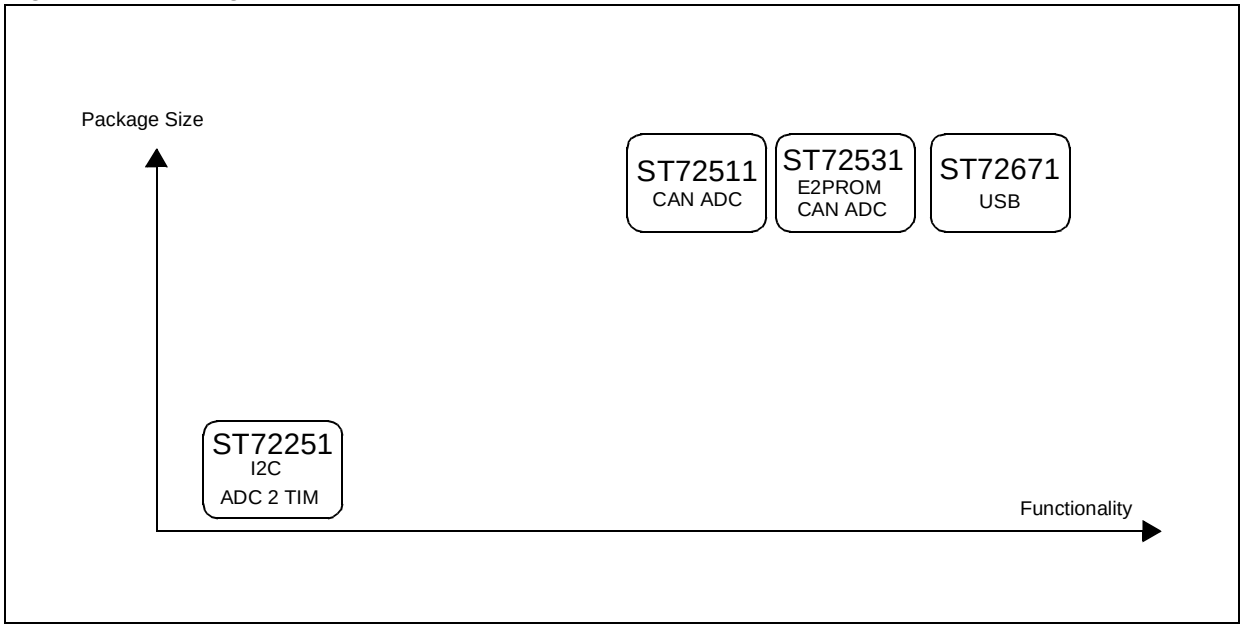
ST7 FAMILY OVERVIEW

The range of six SMD and pin-through packages are available (28, 32, 42, 44, 56 or 64-pin) with a broad mix of on-chip resources giving designers considerable choice when selecting components and determining overall hardware cost.

All devices are available in a wide range of program and data memory sizes. ROM program memory is available for high volume production. On ROM devices the customer's program code is mask programmed by STMicroelectronics during the device manufacture. OTP (One Time Programmable) versions are particularly adapted to small and medium production volumes, as well as to products using different firmware versions or with code that is frequently updated. OTP devices are programmable by the customer using STMicroelectronics or third-party EPROM programmers. EPROM versions can be used during development and prototyping as the program memory can be erased and programmed as often as required.

Available on-chip peripherals include a 16-bit Timer, Watchdog timer, A/D converter, D/A converter, asynchronous communications interface, SPI, I^2C, USB and CAN interfaces. On-chip EEPROM is available on some devices.

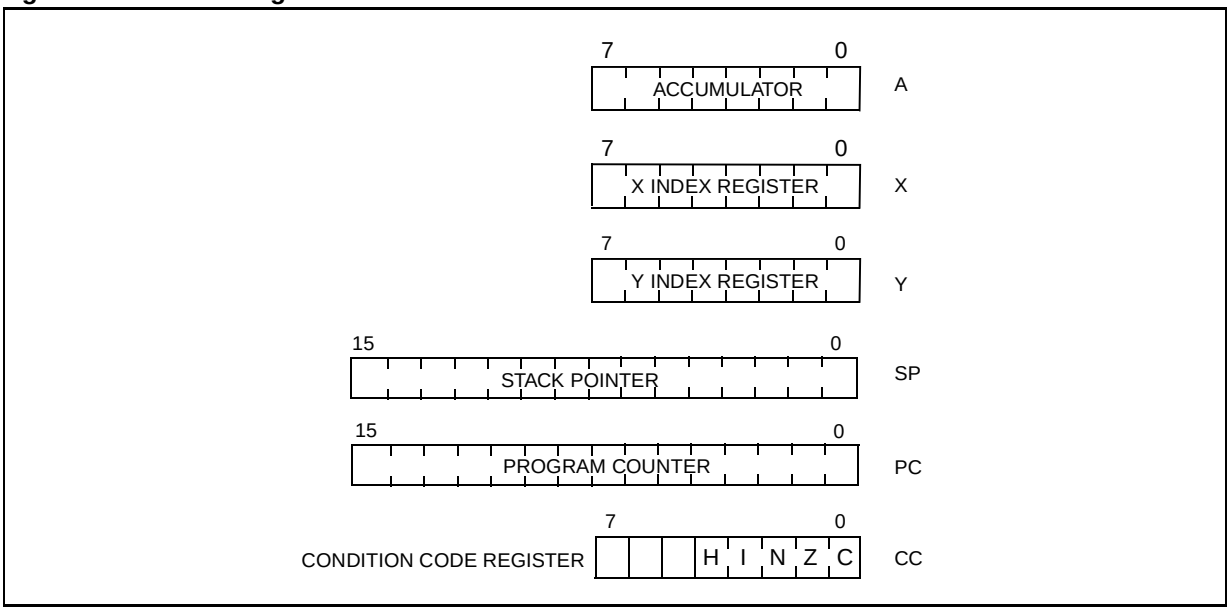
Figure 2. ST7 Integrated Microcontroller Solutions



CPU CORE ARCHITECTURE

The industry-standard 8-bit accumulator-based architecture features 6 internal registers including a 16-bit program counter. The instruction set has 63 instructions with 17 addressing modes offering 8x8 bit unsigned multiply, true bit manipulation, various bit/byte transfer modes and powerful branching logic. Peripheral resources are handled via dedicated interrupts and registers.

Figure 3. ST7 CPU Registers



ON-CHIP PERIPHERALS

Parallel I/O Ports

The bidirectional parallel I/O lines are generally grouped as ports of 8 lines each. The number of I/O lines depends on the specific device pinout. The I/O lines can be shared between other on-chip peripherals (alternate functions) and any general purpose I/O function defined by the application. Data is input and output via data registers (one for each port). Data Direction and Option registers allow each line to be individually configured to the application's requirements.

16-Bit Timer

The 16-bit timer can be used for a wide range of standard timing tasks. It has a 16-bit free running counter with programmable prescaler. Each timer can have up to 2 input capture and 2 output compare pins with associated registers. This allows applications to measure pulse intervals or generate pulse waveforms. Timer overflow and other events are flagged in a status register with optional interrupt generation.

Watchdog Timer

The watchdog timer consists of a 7-bit reloadable downcounter that triggers a device reset if it reaches a predefined value. During normal operation, the application reloads the counter at regular intervals to prevent a reset occurring. By this means, if the application hangs, the condition is automatically cleared by resetting the MCU. The “software watchdog” is enabled by software. The “hardware watchdog” is permanently enabled by hardware.

Analog to Digital Converter

The ADC peripheral multiplexes up to 8 analog input channels. It converts the analog input to 8-bit value using monotonic successive approximation. The analog input voltage must lie within the supply voltage range, which is used as the analog reference.

Digital to Analog Converter

The Digital to Analog converter generates 10-bit pulse width modulated signals with a software programmable duty cycle. These signals with external RC filtering, can be used to replace potentiometers and analog voltage control sources. A 12- bit channel is available on some devices.

Asynchronous Serial Communications

The Serial Communications Interface (SCI) offers a flexible means of full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format. A very wide range of baud rates are available using to dual baud rate generator systems on both receive and transmit channels. Transmitter and receiver circuits are independent and can operate at different baud rates.

SPI Serial Peripheral Interface

The SPI peripheral is a synchronous serial interface for Master and Slave device communications. Single master and multimaster mode systems are supported for communication with external peripherals or other microprocessors. Dedicated registers and interrupts allow full software control and user defined protocols.

USB Interface

The USB is standard serial bus intended primarily for PC peripherals such as monitors, keyboards, joysticks, multimedia devices, scanners, etc. It allows such devices to be connected or removed without rebooting or installing drivers. The ST7 peripheral implements the USB low speed function interface. Data transfer is performed by DMA. The USB peripheral has an integrated 3.3V voltage regulator and a transceiver. Suspend and Resume operations are supported.

I^2C Bus Interface

The I^2C bus is a synchronous serial bus for connecting multiple devices using a data line and a clock line. The ST7 I^2C interface operates in multimaster or slave mode and supports speeds of up to 400 KHz. Bus events (Bus busy, slave address recognised) and error conditions are automatically flagged in peripheral registers and interrupts are optionally generated. The interface supports 7 and 10-bit addressing.

CAN Bus Interface

The Controller Area Network (CAN) protocol is becoming more and more widely accepted in Europe and throughout the world. It enables the creation of networks inside a vehicle or an industrial system with high tolerance to error in noisy environments. The Controller area network peripheral conforms to the CAN Specification 2.0 active and 2.0B passive. The interface has three 10-bit transmit/ receive buffers and two 12-bit message acceptance filters. The Baud rates are programmable up to 1 Mbit/sec.

DEVELOPMENT & SUPPORT

Full Hardware and Software Development Support

A full range of development tools is available, including In-Circuit Emulators, OTP/EPROM programming boards and Gang programmers for each device. Software development tools include Assembly Language and C Language programming suites, as well as a proprietary Windows Debugger and a third party Debugger.

Software Development Tools

A full range of development software tools is available for the ST7 family of Microcontrollers. This currently comprises four principal product groups:

- an Assembly Language suite: "**SOFTWARE TOOLS for the ST7 Family**"
- a proprietary Debugger: "**WGDB7 Windows GNU Debugger for the ST7 Family**"
- a third party C-Language suite: "**HIWARE C TOOLCHAIN for the ST7 Family**"
- a third party Debugger: "**HIWARE SOURCE DEBUGGER for the ST7 Family**"

The available products are listed below, together with the relevant upgrade versions.

Sales Type	Product Name	Description
(*)	Software Tools for the ST7 Family	DOS Macro -Assembler, Linker, Library Archiver and Executable File Formatter for the ST7 Family of MCUs
(*)	WGDB7 Windows GNU Debugger for the ST7 Family	Windows based GNU Debugger for the ST7 Family of MCUs
ST7-SWCHIW/PC Upgrade: ST7-SWCHIW/PC-UP	HIWARE C Toolchain for the ST7 Family	Windows based C Language Toolchain for program development
ST7-SWDHIW/PC Upgrade: ST7-SWDHIW/PC-UP	HIWARE Source Debugger for the ST7 Family	Windows based ST7 Debugger suite

(*) These software suites are supplied as standard issue with the ST7 Emulator.

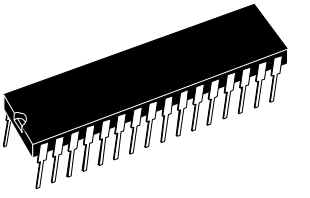
Notes:

ST72101
ST72212/ST72213

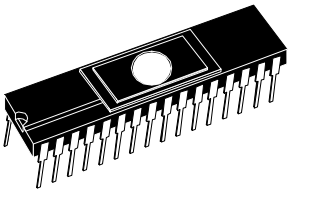
8-BIT MCU WITH 4 TO 8K ROM/OTP/EPROM, 256 BYTES RAM, ADC, WDG, SPI AND 1 OR 2 TIMERS

PRELIMINARY DATA

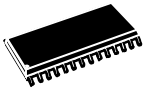
- User Program Memory (ROM/OTP/EPROM): 4 to 8K bytes
- Data RAM: 256 bytes, including 64 bytes of stack
- Master Reset and Power-On Reset
- Run, Wait, Slow, Halt and RAM Retention modes
- 22 multifunctional bidirectional I/O lines:
  - 22 programmable interrupt inputs
  - 8 high sink outputs
  - 6 analog alternate inputs
  - 10 to 14 alternate functions
  - EMI filtering
- Programmable watchdog (WDG)
- One or two 16-bit Timers, each featuring:
  - 2 Input Captures
  - 2 Output Compares
  - External Clock input (on Timer A only)
  - PWM and Pulse Generator modes
- Synchronous Serial Peripheral Interface (SPI)
- 8-bit Analog-to-Digital converter (6 channels) (ST72212 and ST72213 only)
- 8-bit Data Manipulation
- 63 Basic Instructions
- 17 main Addressing Modes
- 8 x 8 Unsigned Multiply Instruction
- True Bit Manipulation
- Complete Development Support on PC/DOS-WINDOWS™ Real-Time Emulator
- Full Software Package on DOS/WINDOWS™ (C-Compiler, Cross-Assembler, Debugger)



PSDIP32



CSDIP32W



PSO28

(See ordering information at the end of datasheet)

Device Summary

Features	ST72101G1	ST72101G2	ST72213G1	ST72212G2
Program Memory- bytes	4K	8K	4K	8K
RAM (stack) - bytes	256 (64)			
16-bit Timers	one	one	one	two
ADC	no	no	yes	yes
Other Peripherals	Watchdog, SPI			
Operating Supply	3 to 6 V			
CPU Frequency	8MH z max (16MHz oscillator)			
Temperature Range	- 40°C to + 85°C			
Package	SO28 - SDIP32			

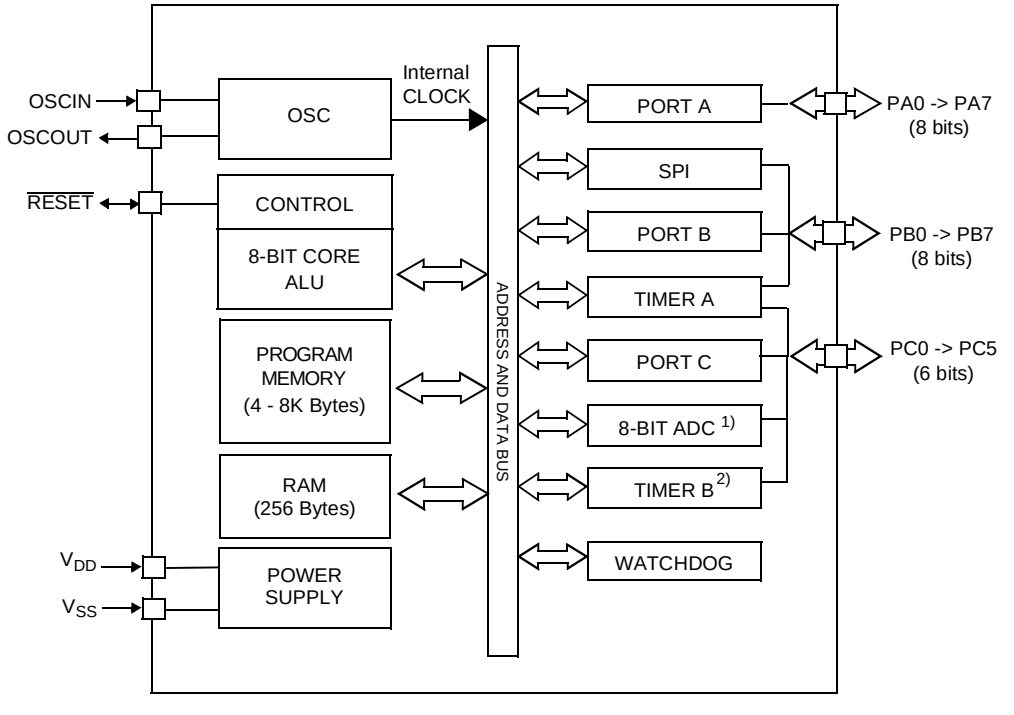
Rev. 1.3

1 GENERAL DESCRIPTION

1.1 INTRODUCTION

The ST72101 ST72213 and ST72212 HCMOS Microcontroller Units are members of the ST7 family. These devices are based on an industry-standard 8-bit core and feature an enhanced instruction set. They normally operate at a 16MHz oscillator frequency. Under software control, the ST72101 ST72213 and ST72212 may be placed in either WAIT, SLOW or HALT modes, thus reducing power consumption. The enhanced instruction set and addressing modes afford real programming potential. In addition to standard 8-bit data management, the ST72101 ST72213 and ST72212 feature true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes on the whole memory. The devices include an on-chip oscillator, CPU, program memory (ROM/OTP/EPROM versions), RAM, 22 I/O lines and the following on-chip peripherals: Analog-to-Digital Converter (ADC) with 6 multiplexed analog inputs (ST72212 and ST72213 only), industry standard synchronous SPI serial interface, digital Watchdog, one or two independent 16-bit Timers, one featuring an External Clock Input, and both featuring Pulse Generator capabilities, 2 Input Captures and 2 Output Compares.

Figure 1. ST72101 ST72213 and ST72212 Block Diagram



1) ST72213 and ST72212 only
2) ST72212 only

1.2 PIN DESCRIPTION

Figure 2. ST72212 Pinout (SO28)

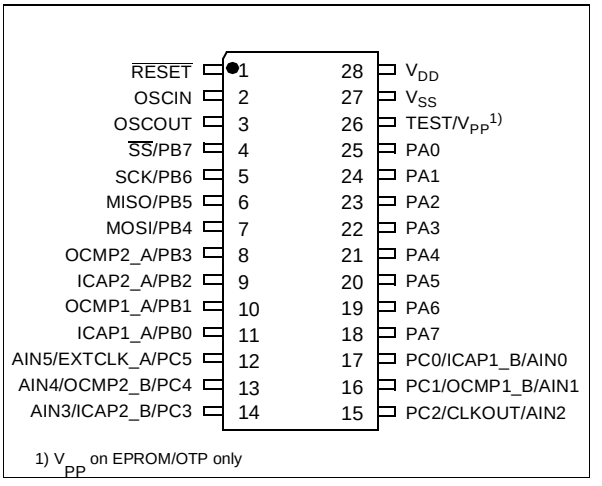


Figure 3. ST72213 Pinout (SO28)

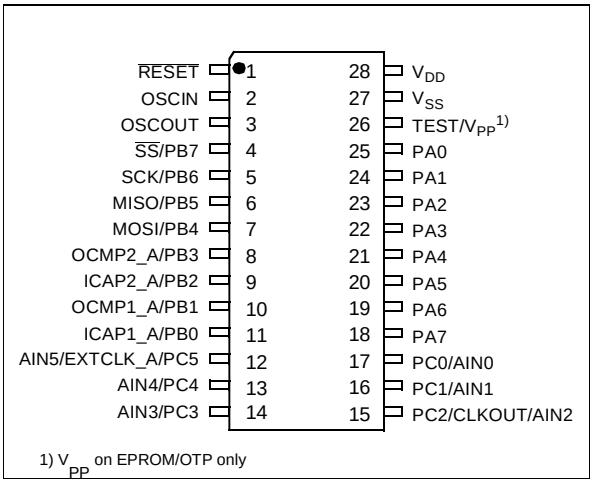


Figure 4. ST72101 Pinout (SO28)

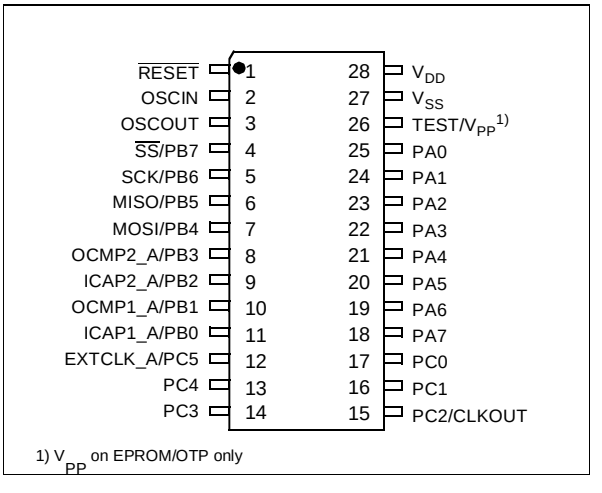


Figure 5. ST72212 Pinout (SDIP32)

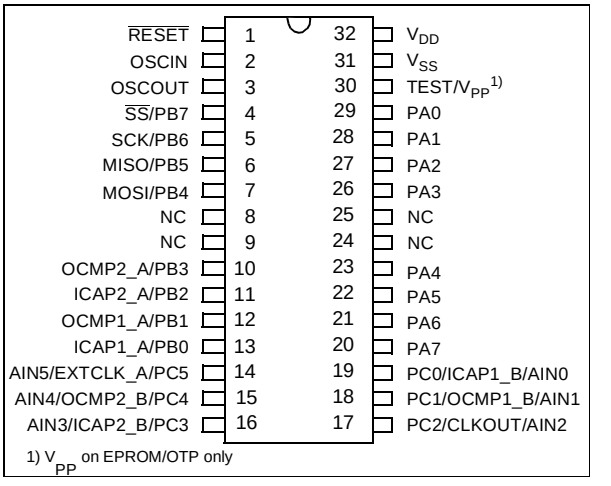


Figure 6. ST72213 Pinout (SDIP32)

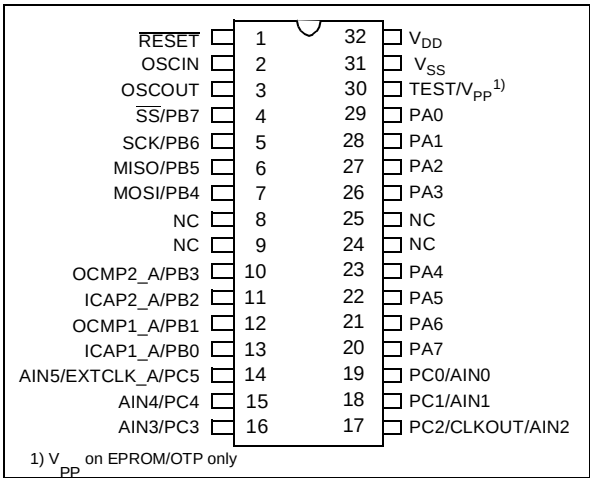


Figure 7. ST72101 Pinout (SDIP32)

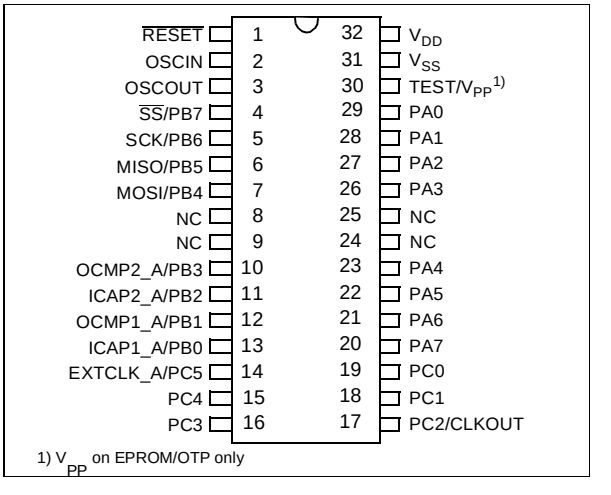


Table 1. ST72212 Pin Configuration

Pin n° SDIP32	Pin n ° SO28	Pin Name	Type	Description	Remarks
1	1	$\overline{\text{RESET}}$	I/O	Bidirectional. Active low. Top priority non maskable interrupt.	
2	2	OSCIN	I	Input/Output Oscillator pin. These pins connect a parallel-resonant crystal, or an external source to the on-chip oscillator.	
3	3	OSCOUT	O		
4	4	PB7/$\overline{\text{SS}}$	I/O	Port B7 or SPI Slave Select (active low)	External Interrupt: EI1
5	5	PB6/SCK	I/O	Port B6 or SPI Serial Clock	External Interrupt: EI1
6	6	PB5/MISO	I/O	Port B5 or SPI Master In/ Slave Out Data	External Interrupt: EI1
7	7	PB4/MOSI	I/O	Port B4 or SPI Master Out / Slave In Data	External Interrupt: EI1
8		NC		Not Connected	
9		NC		Not Connected	
10	8	PB3/OCMP2_A	I/O	Port B3 or TimerA Output Compare 2	External Interrupt: EI1
11	9	PB2/ICAP2_A	I/O	Port B2 or TimerA Input Capture 2	External Interrupt: EI1
12	10	PB1/OCMP1_A	I/O	Port B1 or TimerA Output Compare 1	External Interrupt: EI1
13	11	PB0/ICAP1_A	I/O	Port B0 or TimerA Input Capture 1	External Interrupt: EI1
14	12	PC5/EXTCLK_A/AIN5	I/O	Port C5 or TimerA Input Clock or ADC Analog Input 5	External Interrupt: EI1
15	13	PC4/OCMP2_B/AIN4	I/O	Port C4 or TimerB Output Compare 2 or ADC Analog Input 4	External Interrupt: EI1
16	14	PC3/ICAP2_B/AIN3	I/O	Port C3 or TimerB Input Capture 2 or ADC Analog Input 3	External Interrupt: EI1
17	15	PC2/CLKOUT/AIN2	I/O	Port C2 or Internal Clock Frequency Output or ADC Analog Input 2. Clockout is driven by Bit 5 of the miscellaneous register.	External Interrupt: EI1
18	16	PC1/OCMP1_B/AIN1	I/O	Port C1 or TimerB Output Compare 1 or ADC Analog Input 1	External Interrupt: EI1
19	17	PC0/ICAP1_B/AIN0	I/O	Port C0 or TimerB Input Capture 1 or ADC Analog Input 0	External Interrupt: EI1
20	18	PA7	I/O	Port A7, High Sink	External Interrupt: EI0
21	19	PA6	I/O	Port A6, High Sink	External Interrupt: EI0
22	20	PA5	I/O	Port A5, High Sink	External Interrupt: EI0
23	21	PA4	I/O	Port A4, High Sink	External Interrupt: EI0
24		NC		Not Connected	
25		NC		Not Connected	
26	22	PA3	I/O	Port A3, High Sink	External Interrupt: EI0
27	23	PA2	I/O	Port A2, High Sink	External Interrupt: EI0
28	24	PA1	I/O	Port A1, High Sink	External Interrupt: EI0
29	25	PA0	I/O	Port A0, High Sink	External Interrupt: EI0
30	26	TEST/V_{PP}(1)	S	Test mode pin (should be tied low in user mode). In the EPROM programming mode, this pin acts as the programming voltage input V_{PP}.	
31	27	V_{SS}	S	Ground	
32	28	V_{DD}	S	Main power supply	

Note 1: V_{PP} on EPROM/OTP only

Table 2. ST72213 Pin Configuration

Pin n° SDIP32	Pin n° SO28	Pin Name	Type	Description	Remarks
1	1	$\overline{\text{RESET}}$	I/O	Bidirectional. Active low. Top priority non maskable interrupt.	
2	2	OSCIN	I	Input/Output Oscillator pin. These pins connect a parallel-resonant crystal, or an external source to the on-chip oscillator.	
3	3	OSCOUT	O		
4	4	PB7/$\overline{\text{SS}}$	I/O	Port B7 or SPI Slave Select (active low)	External Interrupt: EI1
5	5	PB6/SCK	I/O	Port B6 or SPI Serial Clock	External Interrupt: EI1
6	6	PB5/MISO	I/O	Port B5 or SPI Master In/ Slave Out Data	External Interrupt: EI1
7	7	PB4/MOSI	I/O	Port B4 or SPI Master Out / Slave In Data	External Interrupt: EI1
8		NC		Not Connected	
9		NC		Not Connected	
10	8	PB3/OCMP2_A	I/O	Port B3 or TimerA Output Compare 2	External Interrupt: EI1
11	9	PB2/ICAP2_A	I/O	Port B2 or TimerA Input Capture 2	External Interrupt: EI1
12	10	PB1/OCMP1_A	I/O	Port B1 or TimerA Output Compare 1	External Interrupt: EI1
13	11	PB0/ICAP1_A	I/O	Port B0 or TimerA Input Capture 1	External Interrupt: EI1
14	12	PC5/EXTCLK_A/AIN5	I/O	Port C5 or TimerA Input Clock or ADC Analog Input 5	External Interrupt: EI1
15	13	PC4/AIN4	I/O	Port C4 or ADC Analog Input 4	External Interrupt: EI1
16	14	PC3/AIN3	I/O	Port C3 or ADC Analog Input 3	External Interrupt: EI1
17	15	PC2/CLKOUT/AIN2	I/O	Port C2 or Internal Clock Frequency Output or ADC Analog Input 2. Clockout is driven by Bit 5 of the miscellaneous register.	External Interrupt: EI1
18	16	PC1/AIN1	I/O	Port C1 or ADC Analog Input 1	External Interrupt: EI1
19	17	PC0/AIN0	I/O	Port C0 or ADC Analog Input 0	External Interrupt: EI1
20	18	PA7	I/O	Port A7, High Sink	External Interrupt: EI0
21	19	PA6	I/O	Port A6, High Sink	External Interrupt: EI0
22	20	PA5	I/O	Port A5, High Sink	External Interrupt: EI0
23	21	PA4	I/O	Port A4, High Sink	External Interrupt: EI0
24		NC		Not Connected	
25		NC		Not Connected	
26	22	PA3	I/O	Port A3, High Sink	External Interrupt: EI0
27	23	PA2	I/O	Port A2, High Sink	External Interrupt: EI0
28	24	PA1	I/O	Port A1, High Sink	External Interrupt: EI0
29	25	PA0	I/O	Port A0, High Sink	External Interrupt: EI0
30	26	TEST/V_{PP}(1)	S	Test mode pin (should be tied low in user mode). In the EPROM programming mode, this pin acts as the programming voltage input V_{PP}.	
31	27	V_{SS}	S	Ground	
32	28	V_{DD}	S	Main power supply	

Note 1: V_{PP} on EPROM/OTP only

Table 3. ST72101 Pin Configuration

Pin n° SDIP32	Pin n° SO28	Pin Name	Type	Description	Remarks
1	1	$\overline{\text{RESET}}$	I/O	Bidirectional. Active low. Top priority non maskable interrupt.	
2	2	OSCIN	I	Input/Output Oscillator pin. These pins connect a parallel-resonant crystal, or an external source to the on-chip oscillator.	
3	3	OSCOUT	O		
4	4	PB7/$\overline{\text{SS}}$	I/O	Port B7 or SPI Slave Select (active low)	External Interrupt: EI1
5	5	PB6/SCK	I/O	Port B6 or SPI Serial Clock	External Interrupt: EI1
6	6	PB5/MISO	I/O	Port B5 or SPI Master In/ Slave Out Data	External Interrupt: EI1
7	7	PB4/MOSI	I/O	Port B4 or SPI Master Out / Slave In Data	External Interrupt: EI1
8		NC		Not Connected	
9		NC		Not Connected	
10	8	PB3/OCMP2_A	I/O	Port B3 or TimerA Output Compare 2	External Interrupt: EI1
11	9	PB2/ICAP2_A	I/O	Port B2 or TimerA Input Capture 2	External Interrupt: EI1
12	10	PB1/OCMP1_A	I/O	Port B1 or TimerA Output Compare 1	External Interrupt: EI1
13	11	PB0/ICAP1_A	I/O	Port B0 or TimerA Input Capture 1	External Interrupt: EI1
14	12	PC5/EXTCLK_A	I/O	Port C5 or TimerA Input Clock	External Interrupt: EI1
15	13	PC4	I/O	Port C4	External Interrupt: EI1
16	14	PC3	I/O	Port C3	External Interrupt: EI1
17	15	PC2/CLKOUT	I/O	Port C2 or Internal Clock Frequency Output. Clockout is driven by MCO bit of the miscellaneous register.	External Interrupt: EI1
18	16	PC1	I/O	Port C1	External Interrupt: EI1
19	17	PC0	I/O	Port C0	External Interrupt: EI1
20	18	PA7	I/O	Port A7, High Sink	External Interrupt: EI0
21	19	PA6	I/O	Port A6, High Sink	External Interrupt: EI0
22	20	PA5	I/O	Port A5, High Sink	External Interrupt: EI0
23	21	PA4	I/O	Port A4, High Sink	External Interrupt: EI0
24		NC		Not Connected	
25		NC		Not Connected	
26	22	PA3	I/O	Port A3, High Sink	External Interrupt: EI0
27	23	PA2	I/O	Port A2, High Sink	External Interrupt: EI0
28	24	PA1	I/O	Port A1, High Sink	External Interrupt: EI0
29	25	PA0	I/O	Port A0, High Sink	External Interrupt: EI0
30	26	TEST/V_{PP}[(1)]	S	Test mode pin (should be tied low in user mode). In the EPROM programming mode, this pin acts as the programming voltage input V_{PP}.	
31	27	V_{SS}	S	Ground	
32	28	V_{DD}	S	Main power supply	

Note 1: V_{PP} on EPROM/OTP only.

1.3 MEMORY MAP

Figure 8. Memory Map

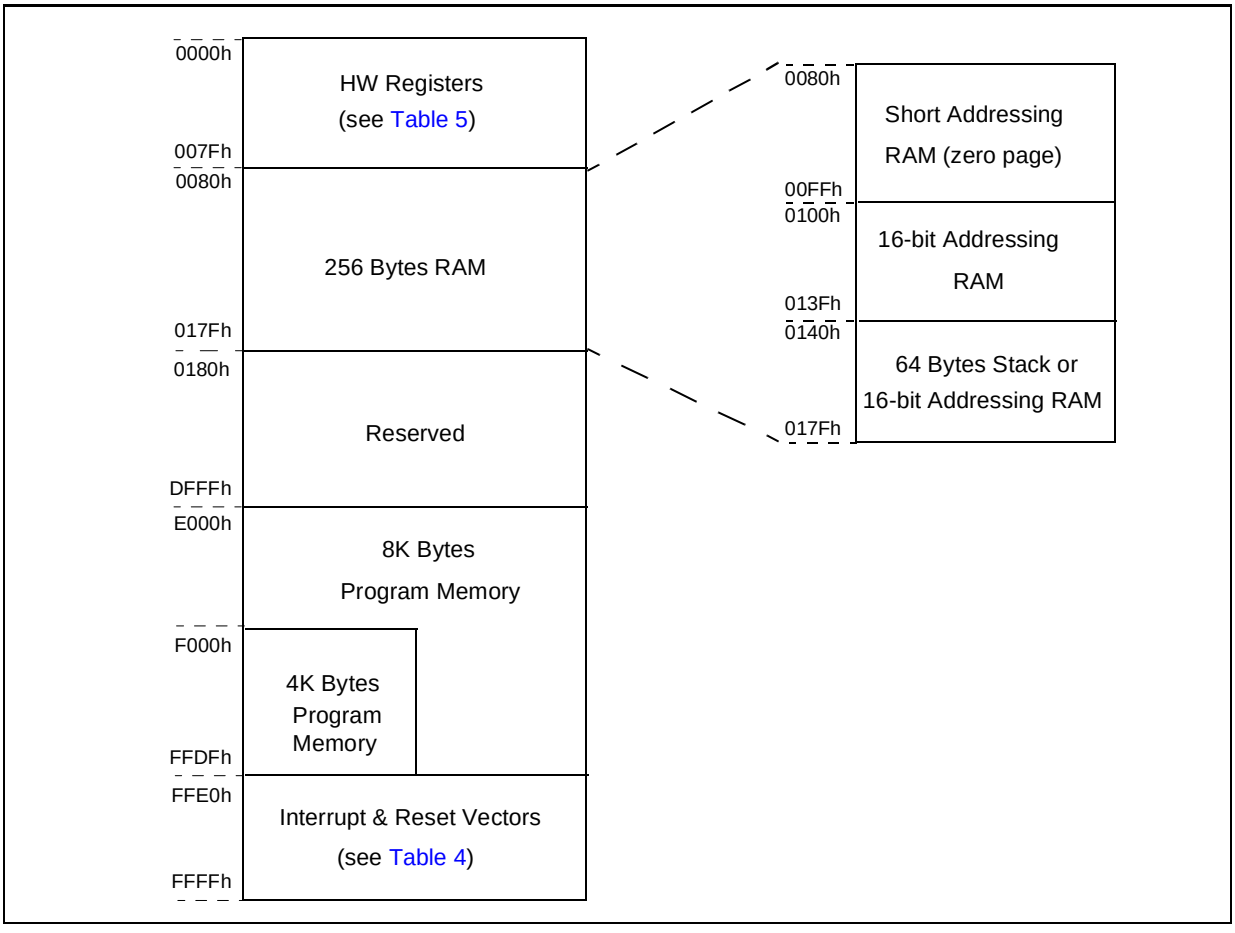


Table 4. Interrupt Vector Map

Vector Address	Description	Remarks
FFE0-FFE1h	Not Used	
FFE2-FFE3h	Not Used	
FFE4-FFE5h	Not Used	
FFE6-FFE7h	Not Used	
FFE8-FFE9h	Not Used	
FFEA-FFEBh	Not Used	
FFEC-FFEDh	Not Used	
FFEE-FFEFh	TIMER B Interrupt Vector (ST72212 only)	Internal Interrupt
FFF0-FFF1h	Not Used	
FFF2-FFF3h	TIMER A Interrupt Vector	Internal Interrupt
FFF4-FFF5h	SPI Interrupt Vector	Internal Interrupt
FFF6-FFF7h	Not Used	
FFF8-FFF9h	External Interrupt Vector EI1	External Interrupt
FFFA-FFFBh	External Interrupt Vector EI0	External Interrupt
FFFC-FFFDh	TRAP (software) Interrupt Vector	CPU Interrupt
FFFE-FFFFh	RESET Vector	

Table 5. Hardware Register Memory Map

Address	Block Name	Register Label	Register name	Reset Status	Remarks
0000h	Port C	PCDR	Data Register	00h	R/W[3]
0001h		PCDDR	Data Direction Register	00h	R/W[3]
0002h		PCOR	Option Register	00h	R/W[3]
0003h	Reserved Area (1 Byte)				
0004h	Port B	PBDR	Data Register	00h	R/W
0005h		PBDDR	Data Direction Register	00h	R/W
0006h		PBOR	Option Register	00h	R/W
0007h	Reserved Area (1 Byte)				
0008h	Port A	PADR	Data Register	00h	R/W
0009h		PADDR	Data Direction Register	00h	R/W
000Ah		PAOR	Option Register	00h	R/W
000Bh to 001Fh	Reserved Area (21 Bytes)				
0020h		MISCR	Miscellaneous Register	00h	R/W
0021h	SPI	SPIDR	Data I/O Register	xxh	R/W
0022h		SPICR	Control Register	0xh	R/W
0023h		SPISR	Status Register	00h	Read Only
0024h	WDG	WDGCR	Watchdog Control register	7Fh	R/W
0025h to 0030h	Reserved Area (12 Bytes)				
0031h	Timer A	TACR2	Control Register2	00h	R/W
0032h		TACR1	Control Register1	00h	R/W
0033h		TASR	Status Register	00h	Read Only
0034h-0035h		TAIC1HR	Input Capture1 High Register	xxh	Read Only
		TAIC1LR	Input Capture1 Low Register	xxh	Read Only
0036h-0037h		TAOC1HR	Output Compare1 High Register	80h	R/W
		TAOC1LR	Output Compare1 Low Register	00h	R/W
0038h-0039h		TACHR	Counter High Register	FFh	Read Only
		TACLR	Counter Low Register	FCh	Read Only
003Ah-003Bh		TAACHR	Alternate Counter High Register	FFh	Read Only
		TAACLR	Alternate Counter Low Register	FCh	Read Only
003Ch-003Dh		TAIC2HR	Input Capture2 High Register	xxh	Read Only
		TAIC2LR	Input Capture2 Low Register	xxh	Read Only
003Eh-003Fh		TAOC2HR	Output Compare2 High Register	80h	R/W
		TAOC2LR	Output Compare2 Low Register	00h	R/W
0040h	Reserved Area (1 Byte)				

Address	Block Name	Register Label	Register name	Reset Status	Remarks
0041h	Timer B [1]	TBCR2	Control Register2	00h	R/W
0042h		TBCR1	Control Register1	00h	R/W
0043h		TBSR	Status Register	00h	Read Only
0044h-0045h		TBIC1HR	Input Capture1 High Register	xxh	Read Only
		TBIC1LR	Input Capture1 Low Register	xxh	Read Only
0046h-0047h		TBOC1HR	Output Compare1 High Register	80h	R/W
		TBOC1LR	Output Compare1 Low Register	00h	R/W
0048h-0049h		TBCHR	Counter High Register	FFh	Read Only
		TBCLR	Counter Low Register	FCh	Read Only
004Ah-004Bh		TBACHR	Alternate Counter High Register	FFh	Read Only
		TBACLR	Alternate Counter Low Register	FCh	Read Only
004Ch-004Dh		TBIC2HR	Input Capture2 High Register	xxh	Read Only
		TBIC2LR	Input Capture2 Low Register	xxh	Read Only
004Eh-004Fh		TBOC2HR	Output Compare2 High Register	80h	R/W
		TBOC2LR	Output Compare2 Low Register	00h	R/W
0050h to 006Fh	Reserved Area (32 Bytes)				
0070h	ADC [2]	ADCDR	Data Register	00h	Read Only
0071h		ADCCSR	Control/Status Register	00h	R/W
0072h to 007Fh	Reserved Area (14 Bytes)				

Notes:

1. ST72212 only, reserved area for other devices.
2. ST72212 and ST72213 only, reserved otherwise.
3. The bits corresponding to unavailable pins are forced to zero by hardware

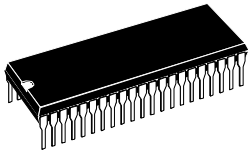
Notes:

ST72121

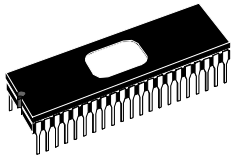
8-BIT MCU WITH 8 TO 16K ROM/OTP/EPROM, 384 TO 512 BYTES RAM, WDG, SCI, SPI AND 2 TIMERS

PRELIMINARY DATA

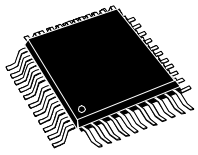
- User Program Memory (ROM/OTP/EPROM): 8 to 16K bytes
- Data RAM: 384 to 512 bytes including 256 bytes of stack
- Master Reset and Power-On Reset
- Low Voltage Detector (LVD) Reset option
- Run and Power Saving modes
- 32 multifunctional bidirectional I/O lines:
  - 9 programmable interrupt inputs
  - 4 high sink outputs
  - 13 alternate functions
  - EMI filtering
- Software or Hardware Watchdog (WDG)
- Two 16-bit Timers, each featuring:
  - 2 Input Captures [1)]
  - 2 Output Compares [1)]
  - External Clock input (on Timer A)
  - PWM and Pulse Generator modes
- Synchronous Serial Peripheral Interface (SPI)
- Asynchronous Serial Communications Interface (SCI)
- 8-bit Data Manipulation
- 63 basic Instructions and 17 main Addressing Modes
- 8 x 8 Unsigned Multiply Instruction
- True Bit Manipulation
- Complete Development Support on DOS/ WINDOWS™ Real-Time Emulator
- Full Software Package on DOS/WINDOWS™ (C-Compiler, Cross-Assembler, Debugger)



PSDIP42



CSDIP42W



TQFP44

Note: 1. One only on Timer A.

Device Summary

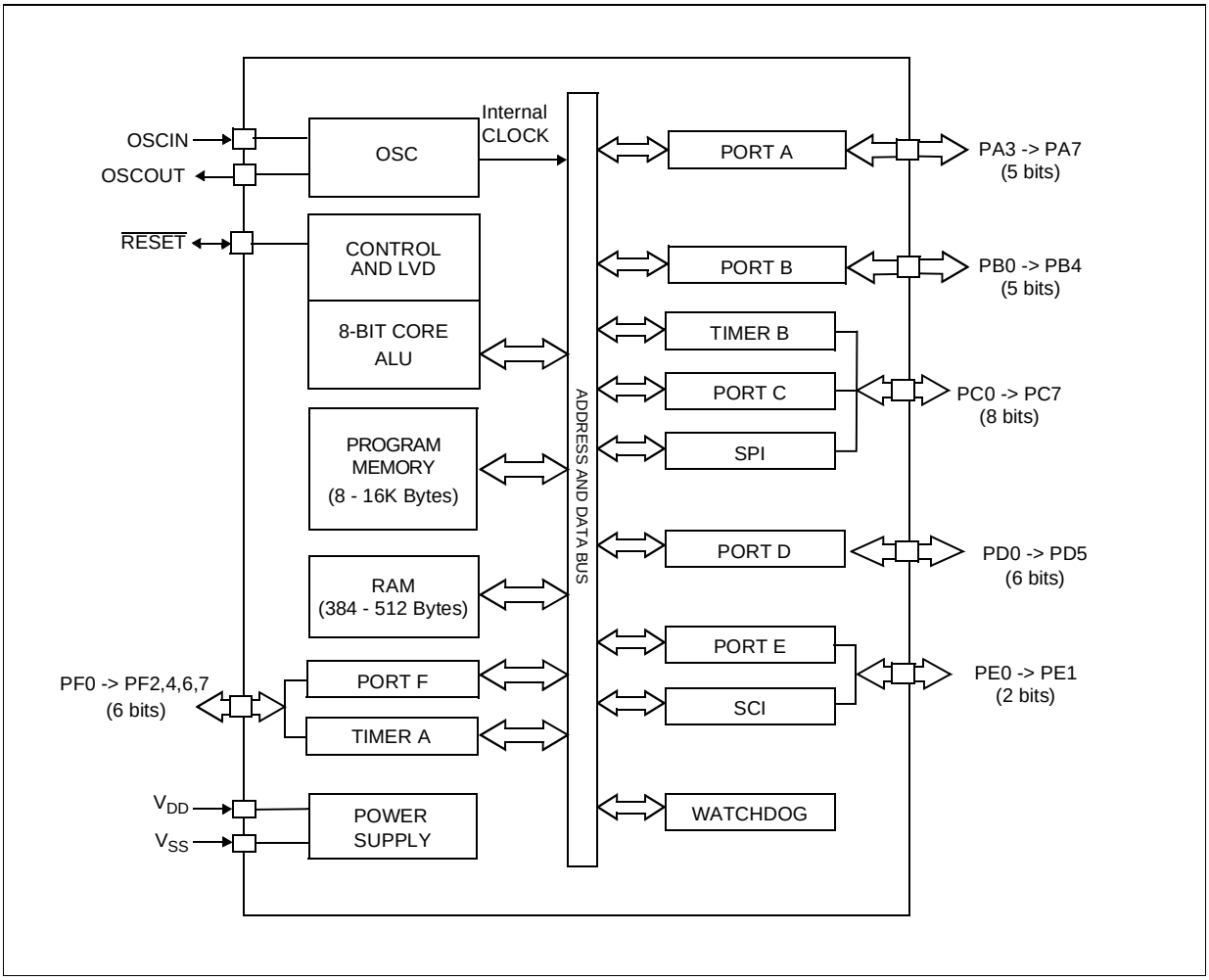
Features	ST72121J2	ST72121J4
Program Memory - bytes	8K	16K
RAM (stack) - bytes	384 (256)	512 (256)
Peripherals	Watchdog, Timers, SPI, SCI and optional Low Voltage Detector Reset	
Operating Supply	3 to 6 V	
CPU Frequency	8 MHz max (16 MHz oscillator)	
Temperature Range	- 40°C to + 85°C	
Package	TQFP44 - SDIP42	
OTP/EPROM Devices	ST72T121J4/ST72E121J4	

1 GENERAL DESCRIPTION

1.1 INTRODUCTION

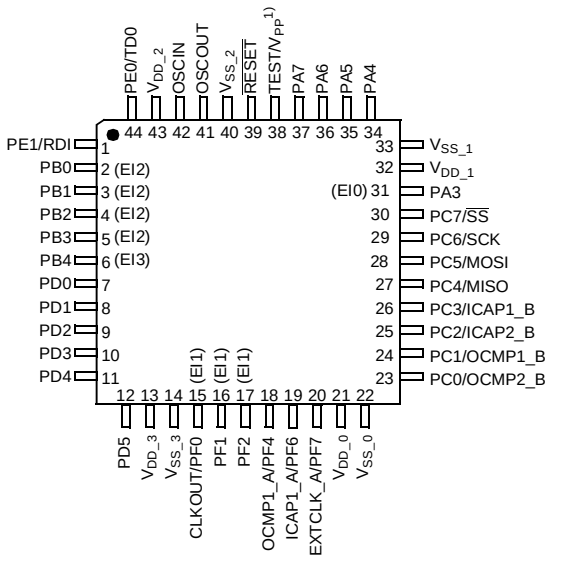
The ST72121 HCMOS Microcontroller Unit (MCU) is a member of the ST7 family. The device is based on an industry-standard 8-bit core and features an enhanced instruction set. The device is normally operated at a 16 MHz oscillator frequency. Under software control, the ST72121 may be placed in either Wait, Slow or Halt modes, thus reducing power consumption. The enhanced instruction set and addressing modes afford real programming potential. In addition to standard 8-bit data management, the ST72121 features true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes on the whole memory. The device includes a low consumption and fast start on-chip oscillator, CPU, program memory (ROM/OTP/EPROM versions), RAM, 32 I/O lines, a Low Voltage Detector (LVD) and the following on-chip peripherals: industry standard synchronous SPI and asynchronous SCI serial interfaces, digital Watchdog, two independent 16-bit Timers, one featuring an External Clock Input, and both featuring Pulse Generator capabilities, 2 Input Captures and 2 Output Compares (only 1 Input Capture and 1 Output Compare on Timer A).

Figure 1. ST72121 Block Diagram



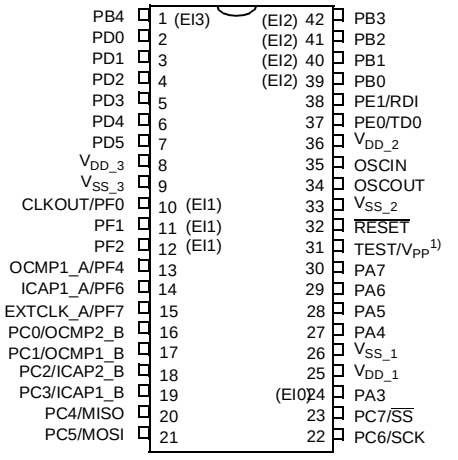
1.2 PIN DESCRIPTION

Figure 2. 44-Pin Thin QFP Package Pinout



1. V_{PP} on EPROM/OTP only

Figure 3. 42-Pin Shrink DIP Package Pinout



1. V_{PP} on EPROM/OTP only

Table 6. ST72121Jx Pin Description

Pin n° QFP44	Pin n° SDIP42	Pin Name	Type	Description	Remarks
1	38	PE1/RDI	I/O	Port E1 or SCI Receive Data In	
2	39	PB0	I/O	Port B0	External Interrupt: EI2
3	40	PB1	I/O	Port B1	External Interrupt: EI2
4	41	PB2	I/O	Port B2	External Interrupt: EI2
5	42	PB3	I/O	Port B3	External Interrupt: EI2
6	1	PB4	I/O	Port B4	External Interrupt: EI3
7	2	PD0	I/O	Port D0	
8	3	PD1	I/O	Port D1	
9	4	PD2	I/O	Port D2	
10	5	PD3	I/O	Port D3	
11	6	PD4	I/O	Port D4	
12	7	PD5	I/O	Port D5	
13	8	V_{DD_3}	S	Main Power Supply	
14	9	V_{SS_3}	S	Ground	
15	10	PF0/CLKOUT	I/O	Port F0 or CPU Clock Output	External Interrupt: EI1
16	11	PF1	I/O	Port F1	External Interrupt: EI1
17	12	PF2	I/O	Port F2	External Interrupt: EI1
18	13	PF4/OCMP1_A	I/O	Port F4 or Timer A Output Compare 1	
19	14	PF6/ICAP1_A	I/O	Port F6 or Timer A Input Capture 1	
20	15	PF7/EXTCLK_A	I/O	Port F7 or External Clock on Timer A	
21		V_{DD_0}	S	Main power supply	
22		V_{SS_0}	S	Ground	
23	16	PC0/OCMP2_B	I/O	Port C0 or Timer B Output Compare 2	
24	17	PC1/OCMP1_B	I/O	Port C1 or Timer B Output Compare 1	
25	18	PC2/ICAP2_B	I/O	Port C2 or Timer B Input Capture 2	
26	19	PC3/ICAP1_B	I/O	Port C3 or Timer B Input Capture 1	
27	20	PC4/MISO	I/O	Port C4 or SPI Master In / Slave Out Data	
28	21	PC5/MOSI	I/O	Port C5 or SPI Master Out / Slave In Data	
29	22	PC6/SCK	I/O	Port C6 or SPI Serial Clock	
30	23	PC7/$\overline{SS}$	I/O	Port C7 or SPI Slave Select	
31	24	PA3	I/O	Port A3	External Interrupt: EI0
32	25	V_{DD_1}	S	Main power supply	
33	26	V_{SS_1}	S	Ground	
34	27	PA4	I/O	Port A4	High Sink
35	28	PA5	I/O	Port A5	High Sink
36	29	PA6	I/O	Port A6	High Sink
37	30	PA7	I/O	Port A7	High Sink
38	31	TEST/V_{PP}[1)]	S	Test mode pin. In the EPROM programming mode, this pin acts as the programming voltage input V_{PP}.	This pin must be tied low in user mode
39	32	$\overline{RESET}$	I/O	Bidirectional. Active low. Top priority non maskable interrupt.	
40	33	V_{SS_2}	S	Ground	
41	34	OSCOUT	O	Input/Output Oscillator pin. These pins connect a parallel-resonant crystal, or an external source to the on-chip oscillator.	
42	35	OSCIN	I		
43	36	V_{DD_2}	S	Main power supply	
44	37	PE0/TDO	I/O	Port E0 or SCI Transmit Data Out	

Note 1: V_{PP} on EPROM/OTP only.

1.3 MEMORY MAP

Figure 4. Program Memory Map

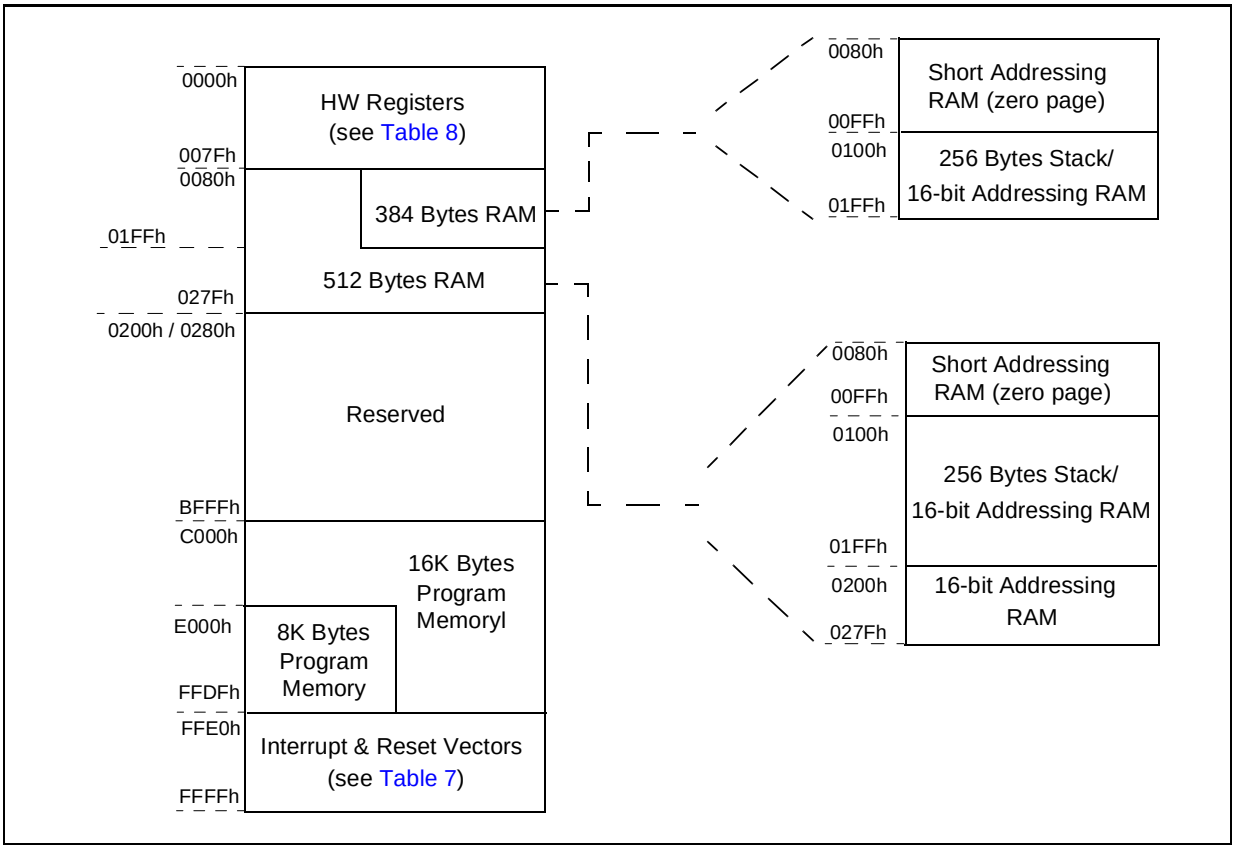


Table 7. Interrupt Vector Map

Vector Address	Description	Remarks
FFE0-FFE1h	Not Used	
FFE2-FFE3h	Not Used	
FFE4-FFE5h	Not Used	Internal Interrupt
FFE6-FFE7h	SCI Interrupt Vector	Internal Interrupt
FFE8-FFE9h	TIMER B Interrupt Vector	Internal Interrupt
FFEA-FFEBh	TIMER A Interrupt Vector	Internal Interrupt
FFEC-FFEDh	SPI interrupt vector	Internal Interrupt
FFEE-FFEFh	Not Used	
FFF0-FFF1h	External Interrupt Vector EI3 (PB4)	External Interrupt
FFF2-FFF3h	External Interrupt Vector EI2 (PB0:PB3)	External Interrupt
FFF4-FFF5h	External Interrupt Vector EI1 (PF0:PF2)	External Interrupt
FFF6-FFF7h	External Interrupt Vector EI0 (PA3)	External Interrupt
FFF8-FFF9h	Not Used	
FFFA-FFFBh	Not Used	
FFFC-FFFDh	TRAP (software) Interrupt Vector	CPU Interrupt
FFFE-FFFFh	RESET Vector	

Table 8. Hardware Register Memory Map

Address	Block	Register Label	Register Name	Reset Status	Remarks
0000h	Port A	PADR	Data Register	00h	R/W
0001h		PADDR	Data Direction Register	00h	R/W
0002h		PAOR	Option Register	00h	R/W [1]
0003h	Reserved Area (1 byte)				
0004h	Port C	PCDR	Data Register	00h	R/W
0005h		PCDDR	Data Direction Register	00h	R/W
0006h		PCOR	Option Register	00h	R/W
0007h	Reserved Area (1 byte)				
0008h	Port B	PBDR	Data Register	00h	R/W
0009h		PBDDR	Data Direction Register	00h	R/W
000Ah		PBOR	Option Register	00h	R/W [1]
000Bh	Reserved Area (1 byte)				
000Ch	Port E	PEDR	Data Register	00h	R/W
000Dh		PEDDR	Data Direction Register	00h	R/W
000Eh		PEOR	Option Register	0Ch	R/W [1]
000Fh	Reserved Area (1 byte)				
0010h	Port D	PDDR	Data Register	00h	R/W
0011h		PDDDR	Data Direction Register	00h	R/W
0012h		PDOR	Option Register	00h	R/W [1]
0013h	Reserved Area (1 byte)				
0014h	Port F	PFDR	Data Register	00h	R/W
0015h		PFDDR	Data Direction Register	00h	R/W
0016h		PFOR	Option Register	28h	R/W [1]
0017h to 001Fh	Reserved Area (9 bytes)				
0020h		MISCR	Miscellaneous Register	00h	
0021h	SPI	SPIDR	SPI Data I/O Register	xxh	R/W
0022h		SPICR	SPI Control Register	xxh	R/W
0023h		SPISR	SPI Status Register	00h	Read Only
0024h to 0029h	Reserved Area (6 bytes)				
002Ah	WDG	WDGCR	Watchdog Control Register	7Fh	R/W
002Bh		WDGSR	Watchdog Status Register	00h	R/W [3]
002Ch to 0030h	Reserved Area (5 bytes)				

Address	Block	Register Label	Register Name	Reset Status	Remarks
0031h		TACR2	Control Register2	00h	R/W
0032h		TACR1	Control Register1	00h	R/W
0033h		TASR	Status Register	xxh	Read Only
0034h-0035h		TAIC1HR	Input Capture1 High Register	xxh	Read Only
		TAIC1LR	Input Capture1 Low Register	xxh	Read Only
0036h-0037h		TAOC1HR	Output Compare1 High Register	80h	R/W
		TAOC1LR	Output Compare1 Low Register	00h	R/W
0038h-0039h	Timer A	TACHR	Counter High Register	FFh	Read Only
		TACLR	Counter Low Register	FCh	Read Only
003Ah-003Bh		TAACHR	Alternate Counter High Register	FFh	Read Only
		TAACLR	Alternate Counter Low Register	FCh	Read Only
003Ch-003Dh		TAIC2HR	Input Capture2 High Register	xxh	Read Only[2]
		TAIC2LR	Input Capture2 Low Register	xxh	Read Only[2]
003Eh-003Fh		TAOC2HR	Output Compare2 High Register	80h	R/W[2]
		TAOC2LR	Output Compare2 Low Register	00h	R/W[2]
0040h	Reserved Area (1 byte)				
0041h		TBCR2	Control Register2	00h	R/W
0042h		TBCR1	Control Register1	00h	R/W
0043h		TBSR	Status Register	xxh	Read Only
0044h-0045h		TBIC1HR	Input Capture1 High Register	xxh	Read Only
		TBIC1LR	Input Capture1 Low Register	xxh	Read Only
0046h-0047h		TBOC1HR	Output Compare1 High Register	80h	R/W
		TBOC1LR	Output Compare1 Low Register	00h	R/W
0048h-0049h	Timer B	TBCHR	Counter High Register	FFh	Read Only
		TBCLR	Counter Low Register	FCh	Read Only
004Ah-004Bh		TBACHR	Alternate Counter High Register	FFh	Read Only
		TBACLR	Alternate Counter Low Register	FCh	Read Only
004Ch-004Dh		TBIC2HR	Input Capture2 High Register	xxh	Read Only
		TBIC2LR	Input Capture2 Low Register	xxh	Read Only
004Eh-004Fh		TBOC2HR	Output Compare2 High Register	80h	R/W
		TBOC2LR	Output Compare2 Low Register	00h	R/W
0050h		SCISR	SCI Status Register	C0h	Read Only
0051h		SCIDR	SCI Data Register	xxh	R/W
0052h		SCIBRR	SCI Baud Rate Register	00x----xb	R/W
0053h	SCI	SCICR1	SCI Control Register 1	xxh	R/W
0054h		SCICR2	SCI Control Register 2	00h	R/W
0055h		SCIERPR	SCI Extended Receive Prescaler Register	00h	R/W
0056h			Reserved	---	Reserved
0057h		SCIETPR	SCI Extended Transmit Prescaler Register	00h	R/W
0058h to 007Fh	Reserved Area (40 bytes)				

Notes:
1. The bits corresponding to unavailable pins are forced to 1 by hardware, this affects the reset status value.
2. External pin not available.
3. Not used in versions without Low Voltage Detector Reset.

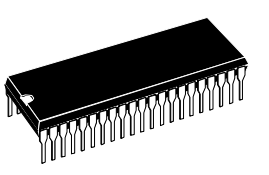
Notes:

ST72311

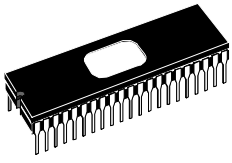
8-BIT MCU WITH 8 TO 16K ROM/OTP/EPROM, 384 TO 512 BYTES RAM, ADC, WDG, SCI, SPI AND 2 TIMERS

PRELIMINARY DATA

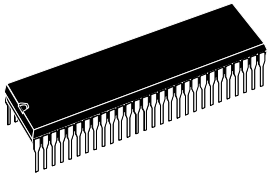
- User Program Memory (ROM/OTP/EPROM): 8 to 16K bytes
- Data RAM: 384 to 512 bytes including 256 bytes of stack
- Master Reset and Power-On Reset
- Low Voltage Detector Reset option
- Run and Power Saving modes
- 44 or 32 multifunctional bidirectional I/O lines:
  - 15 or 9 programmable interrupt inputs
  - 8 or 4 high sink outputs
  - 8 or 6 analog alternate inputs
  - 13 alternate functions
  - EMI filtering
- Software or Hardware Watchdog (WDG)
- Two 16-bit Timers, each featuring:
  - 2 Input Captures [1)]
  - 2 Output Compares [1)]
  - External Clock input (on Timer A)
  - PWM and Pulse Generator modes
- Synchronous Serial Peripheral Interface (SPI)
- Asynchronous Serial Communications Interface (SCI)
- 8-bit ADC with 8 channels [2)]
- 8-bit Data Manipulation
- 63 basic Instructions and 17 main Addressing Modes
- 8 x 8 Unsigned Multiply Instruction
- True Bit Manipulation
- Complete Development Support on DOS/ WINDOWS™ Real-Time Emulator
- Full Software Package on DOS/WINDOWS™ (C-Compiler, Cross-Assembler, Debugger)



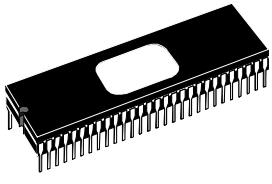
PSDIP42



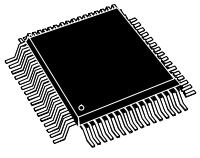
CSDIP42W



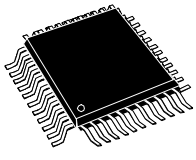
PSDIP56



CSDIP56W



TQFP64



TQFP44

Notes:

1. One only on Timer A.

2. Six channels only for ST72311J.

Device Summary

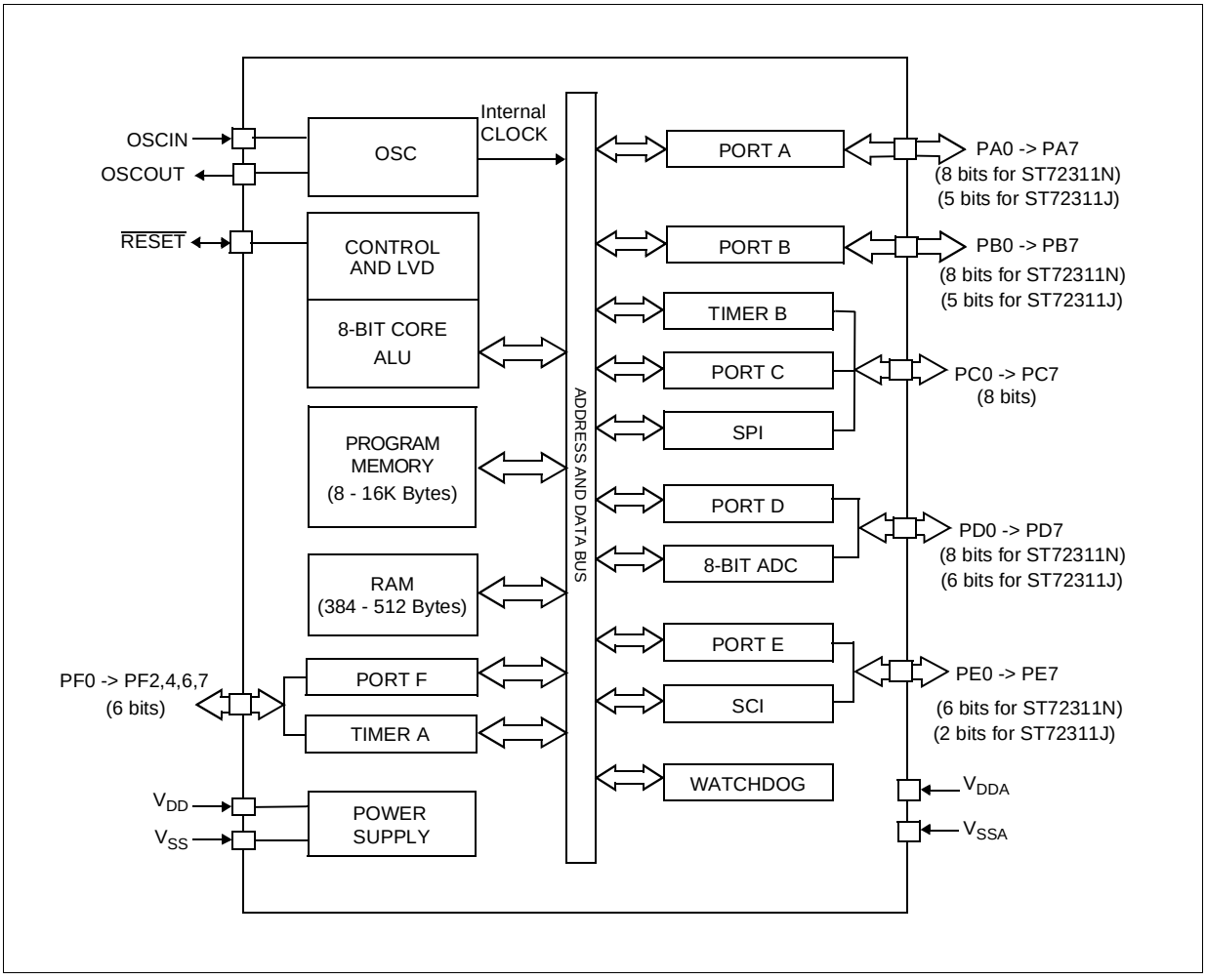
Features	ST72311J2	ST72311J4	ST72311N2	ST72311N4
Program Memory - bytes	8K	16K	8K	16K
RAM (stack) - bytes	384 (256)	512 (256)	384 (256)	512 (256)
Peripherals	Watchdog, Timers, SPI, SCI, ADC and optional Low Voltage Detector Reset			
Operating Supply	3 to 6 V			
CPU Frequency	8 MHz max (16 MHz oscillator)			
Temperature Range	- 40°C to + 85°C			
Package	TQFP44 - SDIP42		TQFP64 - SDIP56	

1 GENERAL DESCRIPTION

1.1 INTRODUCTION

The ST72311 HCMOS Microcontroller Unit (MCU) is a member of the ST7 family. The device is based on an industry-standard 8-bit core and features an enhanced instruction set. The device is normally operated at a 16 MHz oscillator frequency. Under software control, the ST72311 may be placed in either Wait, Slow or Halt modes, thus reducing power consumption. The enhanced instruction set and addressing modes afford real programming potential. In addition to standard 8-bit data management, the ST72311 features true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes on the whole memory. The device includes a low consumption and fast start on-chip oscillator, CPU, program memory (ROM/OTP/EPROM versions), RAM, 44 (ST72311N) or 32 (ST72311J) I/O lines, a Low Voltage Detector (LVD) and the following on-chip peripherals: Analog-to-Digital converter (ADC) with 8 (ST72311N) or 6 (ST72311J) multiplexed analog inputs, industry standard synchronous SPI and asynchronous SCI serial interfaces, digital Watchdog, two independent 16-bit Timers, one featuring an External Clock Input, and both featuring Pulse Generator capabilities, 2 Input Captures and 2 Output Compares (only 1 Input Capture and 1 Output Compare on Timer A).

Figure 1. ST72311 Block Diagram



1.2 PIN DESCRIPTION

Figure 2. 64-Pin Thin QFP Package Pinout

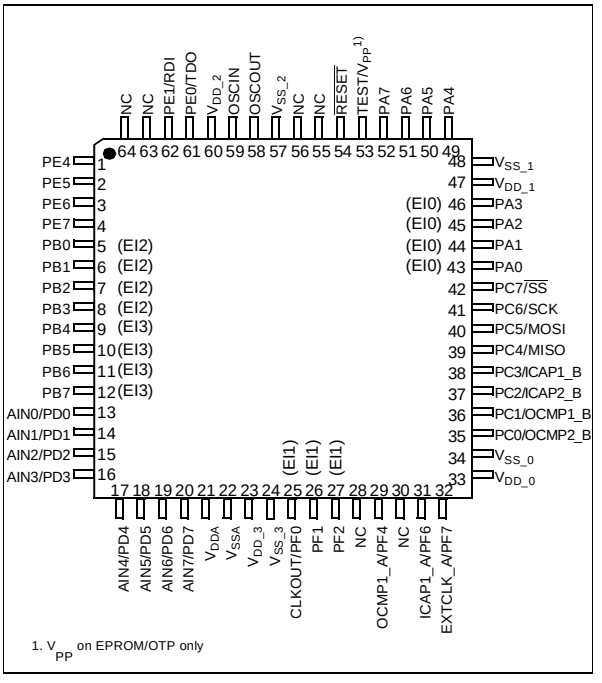


Figure 3. 56-Pin Shrink DIP Package Pinout

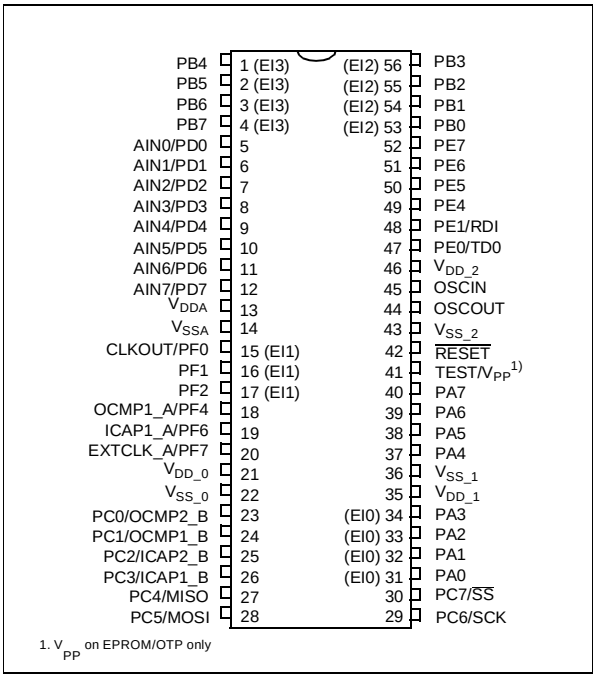


Figure 4. 44-Pin Thin QFP Package Pinout

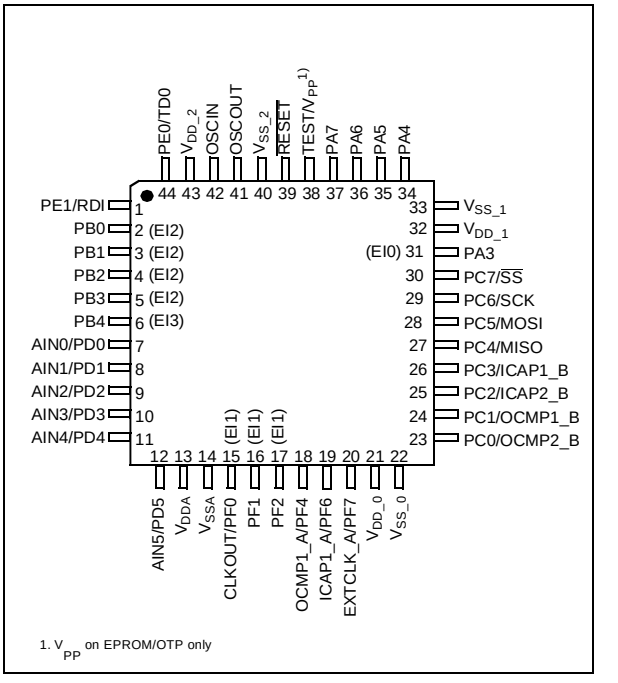


Figure 5. 42-Pin Shrink DIP Package Pinout

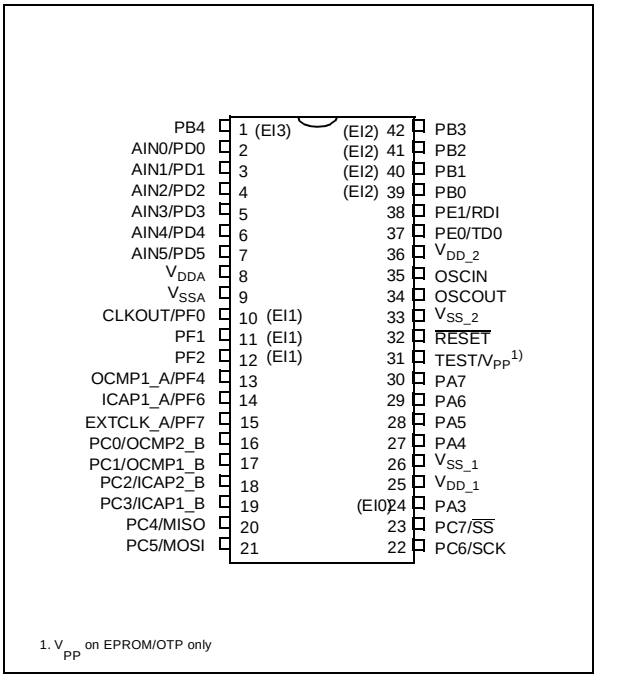


Table 1. ST72311Nx Pin Description

Pin n° QFP64	Pin n° SDIP56	Pin Name	Type	Description	Remarks
1	49	PE4	I/O	Port E4	High Sink
2	50	PE5	I/O	Port E5	High Sink
3	51	PE6	I/O	Port E6	High Sink
4	52	PE7	I/O	Port E7	High Sink
5	53	PB0	I/O	Port B0	External Interrupt: EI2
6	54	PB1	I/O	Port B1	External Interrupt: EI2
7	55	PB2	I/O	Port B2	External Interrupt: EI2
8	56	PB3	I/O	Port B3	External Interrupt: EI2
9	1	PB4	I/O	Port B4	External Interrupt: EI3
10	2	PB5	I/O	Port B5	External Interrupt: EI3
11	3	PB6	I/O	Port B6	External Interrupt: EI3
12	4	PB7	I/O	Port B7	External Interrupt: EI3
13	5	PD0/AIN0	I/O	Port D0 or ADC Analog Input 0	
14	6	PD1/AIN1	I/O	Port D1 or ADC Analog Input 1	
15	7	PD2/AIN2	I/O	Port D2 or ADC Analog Input 2	
16	8	PD3/AIN3	I/O	Port D3 or ADC Analog Input 3	
17	9	PD4/AIN4	I/O	Port D4 or ADC Analog Input 4	
18	10	PD5/AIN5	I/O	Port D5 or ADC Analog Input 5	
19	11	PD6/AIN6	I/O	Port D6 or ADC Analog Input 6	
20	12	PD7/AIN7	I/O	Port D7 or ADC Analog Input 7	
21	13	V_{DDA}	S	Power Supply for analog peripheral (ADC)	
22	14	V_{SSA}	S	Ground for analog peripheral (ADC)	
23		V_{DD_3}	S	Main power supply	
24		V_{SS_3}	S	Ground	
25	15	PF0/CLKOUT	I/O	Port F0 or CPU Clock Output	External Interrupt: EI1
26	16	PF1	I/O	Port F1	External Interrupt: EI1
27	17	PF2	I/O	Port F2	External Interrupt: EI1
28		NC		Not Connected	
29	18	PF4/OCMP1_A	I/O	Port F4 or Timer A Output Compare 1	
30		NC		Not Connected	
31	19	PF6/ICAP1_A	I/O	Port F6 or Timer A Input Capture 1	
32	20	PF7/EXTCLK_A	I/O	Port F7 or External Clock on Timer A	
33	21	V_{DD_0}	S	Main power supply	
34	22	V_{SS_0}	S	Ground	
35	23	PC0/OCMP2_B	I/O	Port C0 or Timer B Output Compare 2	
36	24	PC1/OCMP1_B	I/O	Port C1 or Timer B Output Compare 1	
37	25	PC2/ICAP2_B	I/O	Port C2 or Timer B Input Capture 2	
38	26	PC3/ICAP1_B	I/O	Port C3 or Timer B Input Capture 1	
39	27	PC4/MISO	I/O	Port C4 or SPI Master In / Slave Out Data	
40	28	PC5/MOSI	I/O	Port C5 or SPI Master Out / Slave In Data	
41	29	PC6/SCK	I/O	Port C6 or SPI Serial Clock	
42	30	PC7/$\overline{SS}$	I/O	Port C7 or SPI Slave Select	
43	31	PA0	I/O	Port A0	External Interrupt: EI0

Pin n° QFP64	Pin n° SDIP56	Pin Name	Type	Description	Remarks
44	32	PA1	I/O	Port A1	External Interrupt: EI0
45	33	PA2	I/O	Port A2	External Interrupt: EI0
46	34	PA3	I/O	Port A3	External Interrupt: EI0
47	35	V_{DD_1}	S	Main power supply	
48	36	V_{SS_1}	S	Ground	
49	37	PA4	I/O	Port A4	High Sink
50	38	PA5	I/O	Port A5	High Sink
51	39	PA6	I/O	Port A6	High Sink
52	40	PA7	I/O	Port A7	High Sink
53	41	TEST/V_{PP}[1)]	S	Test mode pin. In the EPROM programming mode, this pin acts as the programming voltage input V_{PP}.	This pin must be tied low in user mode
54	42	$\overline{\text{RESET}}$	I/O	Bidirectional. Active low. Top priority non maskable interrupt.	
55		NC		Not Connected	
56		NC		Not Connected	
57	43	V_{SS_2}	S	Ground	
58	44	OSCOUT	O	Input/Output Oscillator pin. These pins connect a parallel-resonant crystal, or an external source to the on-chip oscillator.	
59	45	OSCIN	I		
60	46	V_{DD_2}	S	Main power supply	
61	47	PE0/TDO	I/O	Port E1 or SCI Transmit Data Out	
62	48	PE1/RDI	I/O	Port E1 or SCI Receive Data In	
63		NC		Not Connected	
64		NC		Not Connected	

Note 1: V_{PP} on EPROM/OTP only.

Table 2. ST72311Jx Pin Description

Pin n° QFP44	Pin n° SDIP42	Pin Name	Type	Description	Remarks
1	38	PE1/RDI	I/O	Port E1 or SCI Receive Data In	
2	39	PB0	I/O	Port B0	External Interrupt: EI2
3	40	PB1	I/O	Port B1	External Interrupt: EI2
4	41	PB2	I/O	Port B2	External Interrupt: EI2
5	42	PB3	I/O	Port B3	External Interrupt: EI2
6	1	PB4	I/O	Port B4	External Interrupt: EI3
7	2	PD0/AIN0	I/O	Port D0 or ADC Analog Input 0	
8	3	PD1/AIN1	I/O	Port D1 or ADC Analog Input 1	
9	4	PD2/AIN2	I/O	Port D2 or ADC Analog Input 2	
10	5	PD3/AIN3	I/O	Port D3 or ADC Analog Input 3	
11	6	PD4/AIN4	I/O	Port D4 or ADC Analog Input 4	
12	7	PD5/AIN5	I/O	Port D5 or ADC Analog Input 5	
13	8	V_{DDA}	S	Power Supply for analog peripheral (ADC)	
14	9	V_{SSA}	S	Ground for analog peripheral (ADC)	
15	10	PF0/CLKOUT	I/O	Port F0 or CPU Clock Output	External Interrupt: EI1
16	11	PF1	I/O	Port F1	External Interrupt: EI1
17	12	PF2	I/O	Port F2	External Interrupt: EI1

Pin n° QFP44	Pin n° SDIP42	Pin Name	Type	Description	Remarks
18	13	PF4/OCMP1_A	I/O	Port F4 or Timer A Output Compare 1	
19	14	PF6/ICAP1_A	I/O	Port F6 or Timer A Input Capture 1	
20	15	PF7/EXTCLK_A	I/O	Port F7 or External Clock on Timer A	
21		V_{DD_0}	S	Main power supply	
22		V_{SS_0}	S	Ground	
23	16	PC0/OCMP2_B	I/O	Port C0 or Timer B Output Compare 2	
24	17	PC1/OCMP1_B	I/O	Port C1 or Timer B Output Compare 1	
25	18	PC2/ICAP2_B	I/O	Port C2 or Timer B Input Capture 2	
26	19	PC3/ICAP1_B	I/O	Port C3 or Timer B Input Capture 1	
27	20	PC4/MISO	I/O	Port C4 or SPI Master In / Slave Out Data	
28	21	PC5/MOSI	I/O	Port C5 or SPI Master Out / Slave In Data	
29	22	PC6/SCK	I/O	Port C6 or SPI Serial Clock	
30	23	PC7/$\overline{SS}$	I/O	Port C7 or SPI Slave Select	
31	24	PA3	I/O	Port A3	External Interrupt: EI0
32	25	V_{DD_1}	S	Main power supply	
33	26	V_{SS_1}	S	Ground	
34	27	PA4	I/O	Port A4	High Sink
35	28	PA5	I/O	Port A5	High Sink
36	29	PA6	I/O	Port A6	High Sink
37	30	PA7	I/O	Port A7	High Sink
38	31	TEST/V_{PP}[1)]	S	Test mode pin. In the EPROM programming mode, this pin acts as the programming voltage input V_{PP}.	This pin must be tied low in user mode
39	32	$\overline{RESET}$	I/O	Bidirectional. Active low. Top priority non maskable interrupt.	
40	33	V_{SS_2}	S	Ground	
41	34	OSCOUT	O	Input/Output Oscillator pin. These pins connect a parallel-resonant crystal, or an external source to the on-chip oscillator.	
42	35	OSCIN	I		
43	36	V_{DD_2}	S	Main power supply	
44	37	PE0/TDO	I/O	Port E0 or SCI Transmit Data Out	

Note 1: V_{PP} on EPROM/OTP only.

1.3 MEMORY MAP

Figure 6. Program Memory Map

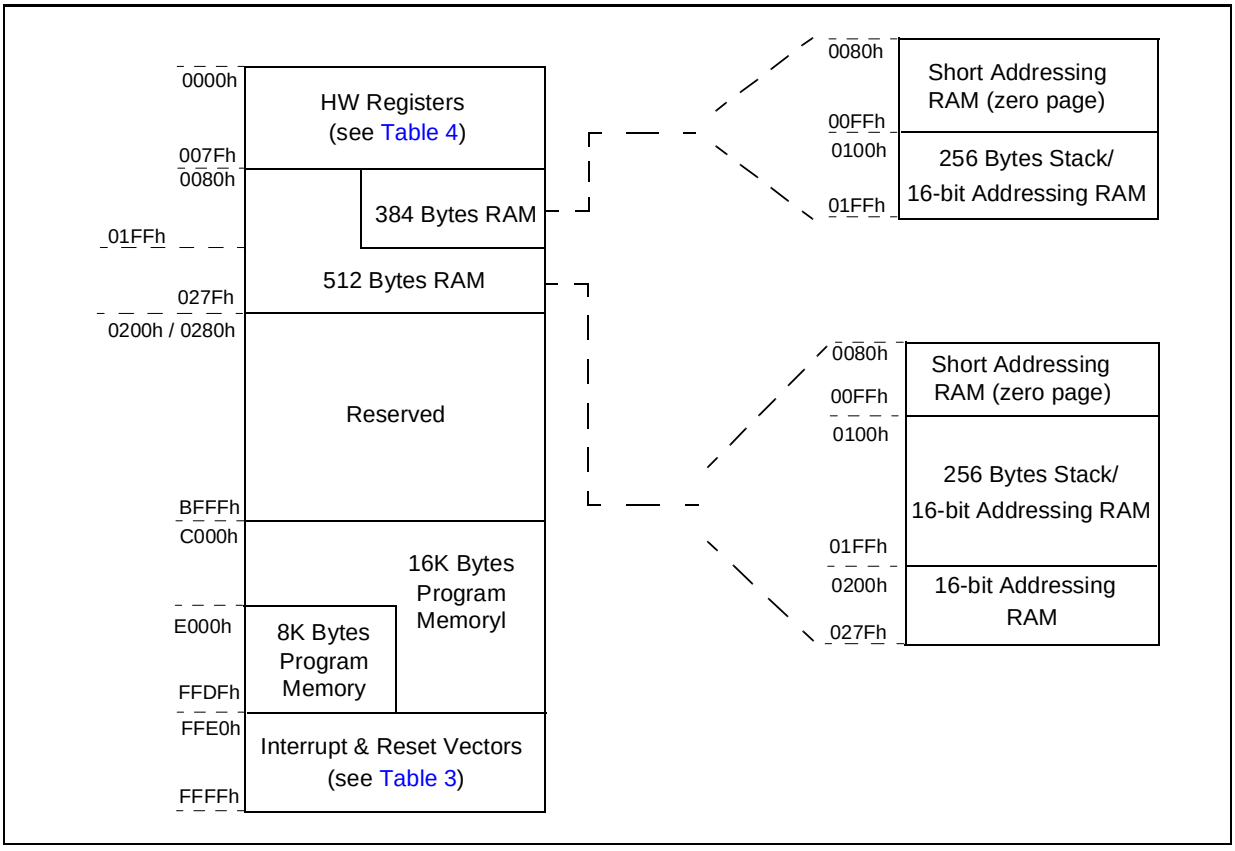


Table 3. Interrupt Vector Map

Vector Address	Description	Remarks
FFE0-FFE1h	Not Used	
FFE2-FFE3h	Not Used	
FFE4-FFE5h	Not Used	Internal Interrupt
FFE6-FFE7h	SCI Interrupt Vector	Internal Interrupt
FFE8-FFE9h	TIMER B Interrupt Vector	Internal Interrupt
FFEA-FFEBh	TIMER A Interrupt Vector	Internal Interrupt
FFEC-FFEDh	SPI interrupt vector	Internal Interrupt
FFEE-FFEFh	Not Used	
FFF0-FFF1h	External Interrupt Vector EI3	External Interrupt
FFF2-FFF3h	External Interrupt Vector EI2	External Interrupt
FFF4-FFF5h	External Interrupt Vector EI1	External Interrupt
FFF6-FFF7h	External Interrupt Vector EI0	External Interrupt
FFF8-FFF9h	Not Used	
FFFA-FFFBh	Not Used	
FFFC-FFFDh	TRAP (software) Interrupt Vector	CPU Interrupt
FFFE-FFFFh	RESET Vector	

Table 4. Hardware Register Memory Map

Address	Block	Register Label	Register Name	Reset Status	Remarks
0000h	Port A	PADR	Data Register	00h	R/W
0001h		PADDR	Data Direction Register	00h	R/W
0002h		PAOR	Option Register	00h	R/W [1]
0003h	Reserved Area (1 byte)				
0004h	Port C	PCDR	Data Register	00h	R/W
0005h		PCDDR	Data Direction Register	00h	R/W
0006h		PCOR	Option Register	00h	R/W
0007h	Reserved Area (1 byte)				
0008h	Port B	PBDR	Data Register	00h	R/W
0009h		PBDDR	Data Direction Register	00h	R/W
000Ah		PBOR	Option Register	00h	R/W [1]
000Bh	Reserved Area (1 byte)				
000Ch	Port E	PEDR	Data Register	00h	R/W
000Dh		PEDDR	Data Direction Register	00h	R/W
000Eh		PEOR	Option Register	0Ch	R/W [1]
000Fh	Reserved Area (1 byte)				
0010h	Port D	PDDR	Data Register	00h	R/W
0011h		PDDDR	Data Direction Register	00h	R/W
0012h		PDOR	Option Register	00h	R/W [1]
0013h	Reserved Area (1 byte)				
0014h	Port F	PFDR	Data Register	00h	R/W
0015h		PFDDR	Data Direction Register	00h	R/W
0016h		PFOR	Option Register	28h	R/W [1]
0017h to 001Fh	Reserved Area (9 bytes)				
0020h		MISCR	Miscellaneous Register	00h	
0021h	SPI	SPIDR	SPI Data I/O Register	xxh	R/W
0022h		SPICR	SPI Control Register	xxh	R/W
0023h		SPISR	SPI Status Register	00h	Read Only
0024h to 0029h	Reserved Area (6 bytes)				
002Ah	WDG	WDGCR	Watchdog Control Register	7Fh	R/W
002Bh		WDGSR	Watchdog Status Register	00h	R/W [3]
002Ch to 0030h	Reserved Area (5 bytes)				

Address	Block	Register Label	Register Name	Reset Status	Remarks
0031h		TACR2	Control Register2	00h	R/W
0032h		TACR1	Control Register1	00h	R/W
0033h		TASR	Status Register	xxh	Read Only
0034h-0035h		TAIC1HR	Input Capture1 High Register	xxh	Read Only
		TAIC1LR	Input Capture1 Low Register	xxh	Read Only
0036h-0037h		TAOC1HR	Output Compare1 High Register	80h	R/W
		TAOC1LR	Output Compare1 Low Register	00h	R/W
0038h-0039h	Timer A	TACHR	Counter High Register	FFh	Read Only
		TACLR	Counter Low Register	FCh	Read Only
003Ah-003Bh		TAACHR	Alternate Counter High Register	FFh	Read Only
		TAACLR	Alternate Counter Low Register	FCh	Read Only
003Ch-003Dh		TAIC2HR	Input Capture2 High Register	xxh	Read Only[2]
		TAIC2LR	Input Capture2 Low Register	xxh	Read Only[2]
003Eh-003Fh		TAOC2HR	Output Compare2 High Register	80h	R/W[2]
		TAOC2LR	Output Compare2 Low Register	00h	R/W[2]
0040h	Reserved Area (1 byte)				
0041h		TBCR2	Control Register2	00h	R/W
0042h		TBCR1	Control Register1	00h	R/W
0043h		TBSR	Status Register	xxh	Read Only
0044h-0045h		TBIC1HR	Input Capture1 High Register	xxh	Read Only
		TBIC1LR	Input Capture1 Low Register	xxh	Read Only
0046h-0047h		TBOC1HR	Output Compare1 High Register	80h	R/W
		TBOC1LR	Output Compare1 Low Register	00h	R/W
0048h-0049h	Timer B	TBCHR	Counter High Register	FFh	Read Only
		TBCLR	Counter Low Register	FCh	Read Only
004Ah-004Bh		TBACHR	Alternate Counter High Register	FFh	Read Only
		TBACLR	Alternate Counter Low Register	FCh	Read Only
004Ch-004Dh		TBIC2HR	Input Capture2 High Register	xxh	Read Only
		TBIC2LR	Input Capture2 Low Register	xxh	Read Only
004Eh-004Fh		TBOC2HR	Output Compare2 High Register	80h	R/W
		TBOC2LR	Output Compare2 Low Register	00h	R/W
0050h		SCISR	SCI Status Register	C0h	Read Only
0051h		SCIDR	SCI Data Register	xxh	R/W
0052h		SCIBRR	SCI Baud Rate Register	00x----xb	R/W
0053h	SCI	SCICR1	SCI Control Register 1	xxh	R/W
0054h		SCICR2	SCI Control Register 2	00h	R/W
0055h		SCIERPR	SCI Extended Receive Prescaler Register	00h	R/W
0056h			Reserved	---	Reserved
0057h		SCIETPR	SCI Extended Transmit Prescaler Register	00h	R/W
0058h to 006Fh	Reserved Area (24 bytes)				
0070h	ADC	ADCDR	ADC Data Register	00h	Read Only
0071h		ADCCSR	ADC Control/Status Register	00h	R/W
0072h to 007Fh	Reserved Area (14 bytes)				

Notes:
1. The bits corresponding to unavailable pins are forced to 1 by hardware, this affects the reset status value.
2. External pin not available.
3. Not used in versions without Low Voltage Detector Reset.

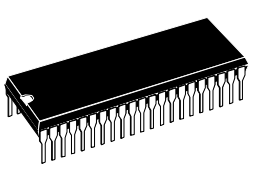
Notes:

ST72331

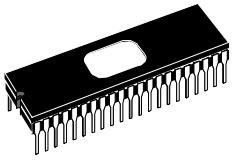
8-BIT MCU WITH 8 TO 16K ROM/OTP/EPROM, 256 EEPROM, 384 TO 512 BYTES RAM, ADC, WDG, SCI, SPI AND 2 TIMERS

PRELIMINARY DATA

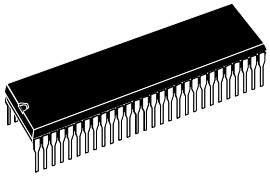
- User Program Memory (ROM/OTP/EPROM): 8 to 16K bytes
- User EEPROM: 256 bytes
- Data RAM: 384 to 512 bytes including 256 bytes of stack
- Master Reset and Power-On Reset
- Low Voltage Detector Reset option
- Run and Power Saving modes
- 44 or 32 multifunctional bidirectional I/O lines:
  - 15 or 9 programmable interrupt inputs
  - 8 or 4 high sink outputs
  - 8 or 6 analog alternate inputs
  - 13 alternate functions
  - EMI filtering
- Software or Hardware Watchdog (WDG)
- Two 16-bit Timers, each featuring:
  - 2 Input Captures [1)]
  - 2 Output Compares [1)]
  - External Clock input (on Timer A)
  - PWM and Pulse Generator modes
- Synchronous Serial Peripheral Interface (SPI)
- Asynchronous Serial Communications Interface (SCI)
- 8-bit ADC with 8 channels [2)]
- 8-bit Data Manipulation
- 63 basic Instructions and 17 main Addressing Modes
- 8 x 8 Unsigned Multiply Instruction
- True Bit Manipulation
- Complete Development Support on DOS/ WINDOWS™ Real-Time Emulator
- Full Software Package on DOS/WINDOWS™ (C-Compiler, Cross-Assembler, Debugger)



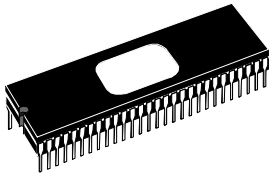
PSDIP42



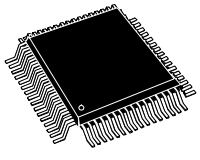
CSDIP42W



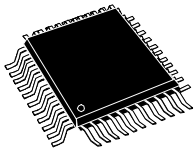
PSDIP56



CSDIP56W



TQFP64



TQFP44

Notes:

1. One only on Timer A.

2. Six channels only for ST72331J.

Device Summary

Features	ST72331J2	ST72331J4	ST72331N2	ST72331N4
Program Memory - bytes	8K	16K	8K	16K
EEPROM - bytes	256			
RAM (stack) - bytes	384 (256)	512 (256)	384 (256)	512 (256)
Peripherals	Watchdog, Timers, SPI, SCI, ADC and optional Low Voltage Detector Reset			
Operating Supply	3 to 6 V			
CPU Frequency	8 MHz max (16 MHz oscillator)			
Temperature Range	- 40°C to + 85°C			
Package	TQFP44 - SDIP42		TQFP64 - SDIP56	

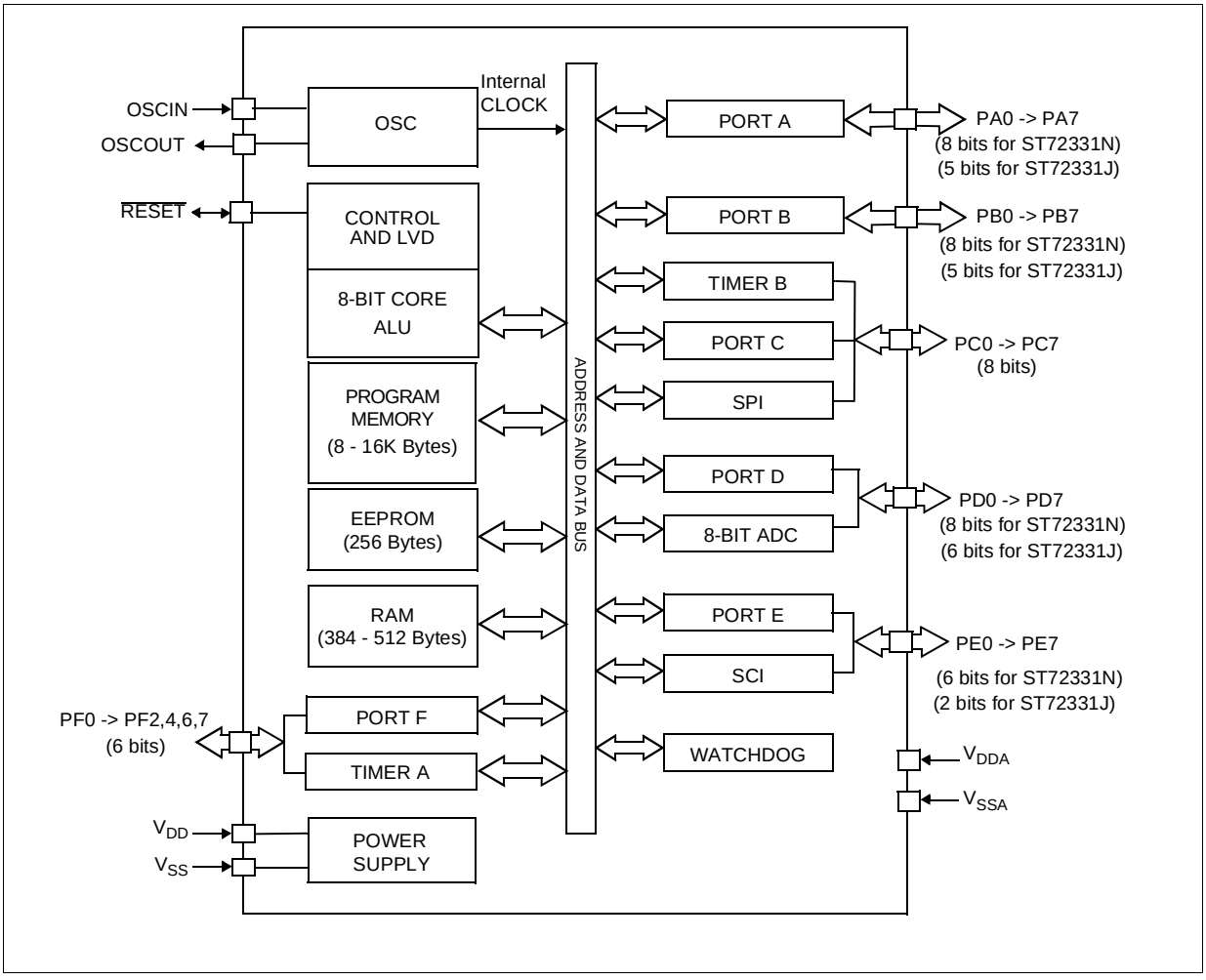
Rev. 1.3

1 GENERAL DESCRIPTION

1.1 INTRODUCTION

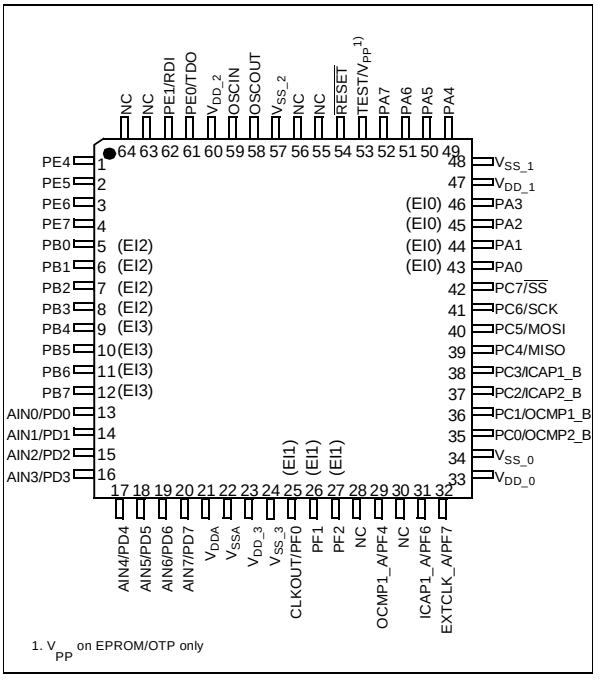
The ST72331 HCMOS Microcontroller Unit (MCU) is a member of the ST7 family. The device is based on an industry-standard 8-bit core and features an enhanced instruction set. The device is normally operated at a 16 MHz oscillator frequency. Under software control, the ST72331 may be placed in either Wait, Slow or Halt modes, thus reducing power consumption. The enhanced instruction set and addressing modes afford real programming potential. In addition to standard 8-bit data management, the ST72331 features true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes on the whole memory. The device includes a low consumption and fast start on-chip oscillator, CPU, program memory (ROM/OTP/EPROM versions), EEPROM, RAM, 44 (QFP64 and SDIP56) or 32 (QFP44 and SDIP42) I/O lines, a Low Voltage Detector (LVD) and the following on-chip peripherals: Analog-to-Digital converter (ADC) with 8 (QFP64, SDIP56) or 6 (QFP44, SDIP42) multiplexed analog inputs, industry standard synchronous SPI and asynchronous SCI serial interfaces, digital Watchdog, two independent 16-bit Timers, one featuring an External Clock Input, and both featuring Pulse Generator capabilities, 2 Input Captures and 2 Output Compares (only 1 Input Capture and 1 Output Compare on Timer A).

Figure 1. ST72331 Block Diagram



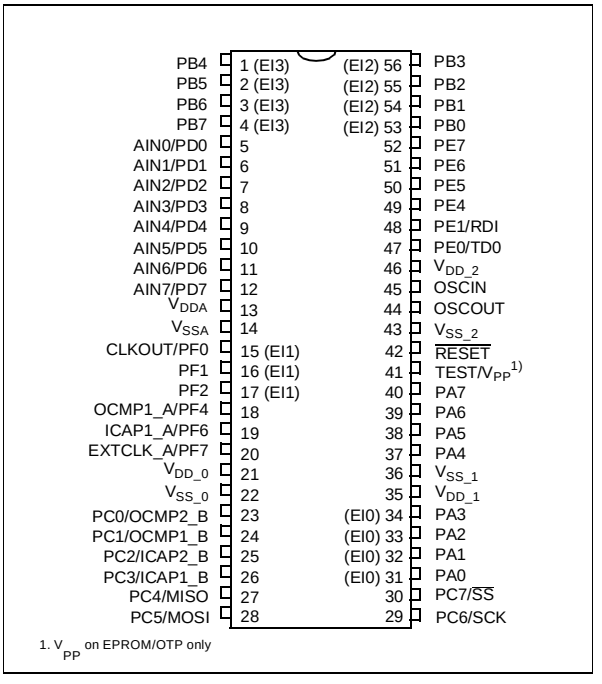
1.2 PIN DESCRIPTION

Figure 2. 64-Pin Thin QFP Package Pinout



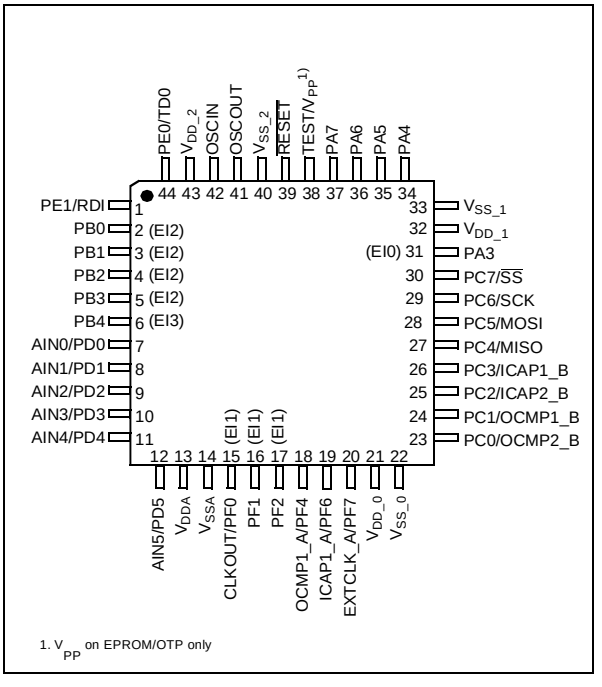
1. V_{PP} on EPROM/OTP only

Figure 3. 56-Pin Shrink DIP Package Pinout



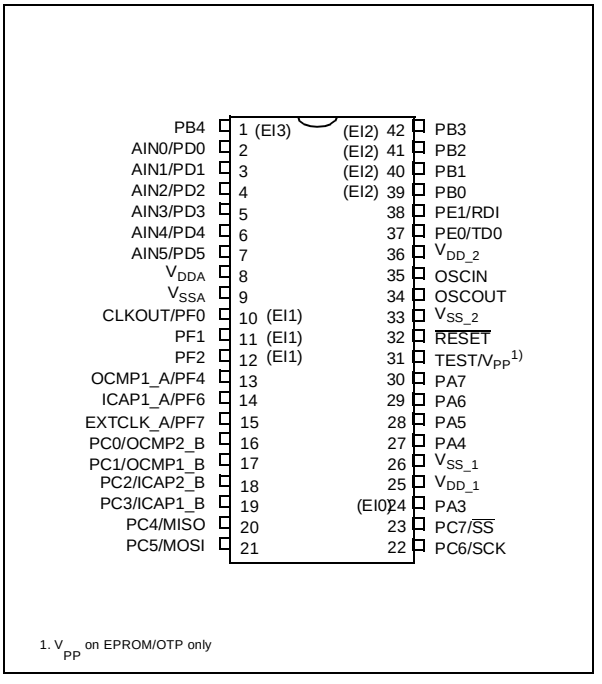
1. V_{PP} on EPROM/OTP only

Figure 4. 44-Pin Thin QFP Package Pinout



1. V_{PP} on EPROM/OTP only

Figure 5. 42-Pin Shrink DIP Package Pinout



1. V_{PP} on EPROM/OTP only

Table 1. ST72331Nx Pin Description

Pin n° QFP64	Pin n° SDIP56	Pin Name	Type	Description	Remarks
1	49	PE4	I/O	Port E4	High Sink
2	50	PE5	I/O	Port E5	High Sink
3	51	PE6	I/O	Port E6	High Sink
4	52	PE7	I/O	Port E7	High Sink
5	53	PB0	I/O	Port B0	External Interrupt: EI2
6	54	PB1	I/O	Port B1	External Interrupt: EI2
7	55	PB2	I/O	Port B2	External Interrupt: EI2
8	56	PB3	I/O	Port B3	External Interrupt: EI2
9	1	PB4	I/O	Port B4	External Interrupt: EI3
10	2	PB5	I/O	Port B5	External Interrupt: EI3
11	3	PB6	I/O	Port B6	External Interrupt: EI3
12	4	PB7	I/O	Port B7	External Interrupt: EI3
13	5	PD0/AIN0	I/O	Port D0 or ADC Analog Input 0	
14	6	PD1/AIN1	I/O	Port D1 or ADC Analog Input 1	
15	7	PD2/AIN2	I/O	Port D2 or ADC Analog Input 2	
16	8	PD3/AIN3	I/O	Port D3 or ADC Analog Input 3	
17	9	PD4/AIN4	I/O	Port D4 or ADC Analog Input 4	
18	10	PD5/AIN5	I/O	Port D5 or ADC Analog Input 5	
19	11	PD6/AIN6	I/O	Port D6 or ADC Analog Input 6	
20	12	PD7/AIN7	I/O	Port D7 or ADC Analog Input 7	
21	13	V_{DDA}	S	Power Supply for analog peripheral (ADC)	
22	14	V_{SSA}	S	Ground for analog peripheral (ADC)	
23		V_{DD_3}	S	Main power supply	
24		V_{SS_3}	S	Ground	
25	15	PF0/CLKOUT	I/O	Port F0 or CPU Clock Output	External Interrupt: EI1
26	16	PF1	I/O	Port F1	External Interrupt: EI1
27	17	PF2	I/O	Port F2	External Interrupt: EI1
28		NC		Not Connected	
29	18	PF4/OCMP1_A	I/O	Port F4 or Timer A Output Compare 1	
30		NC		Not Connected	
31	19	PF6/ICAP1_A	I/O	Port F6 or Timer A Input Capture 1	
32	20	PF7/EXTCLK_A	I/O	Port F7 or External Clock on Timer A	
33	21	V_{DD_0}	S	Main power supply	
34	22	V_{SS_0}	S	Ground	
35	23	PC0/OCMP2_B	I/O	Port C0 or Timer B Output Compare 2	
36	24	PC1/OCMP1_B	I/O	Port C1 or Timer B Output Compare 1	
37	25	PC2/ICAP2_B	I/O	Port C2 or Timer B Input Capture 2	
38	26	PC3/ICAP1_B	I/O	Port C3 or Timer B Input Capture 1	
39	27	PC4/MISO	I/O	Port C4 or SPI Master In / Slave Out Data	
40	28	PC5/MOSI	I/O	Port C5 or SPI Master Out / Slave In Data	
41	29	PC6/SCK	I/O	Port C6 or SPI Serial Clock	
42	30	PC7/$\overline{SS}$	I/O	Port C7 or SPI Slave Select	
43	31	PA0	I/O	Port A0	External Interrupt: EI0

Pin n° QFP64	Pin n° SDIP56	Pin Name	Type	Description	Remarks
44	32	PA1	I/O	Port A1	External Interrupt: EI0
45	33	PA2	I/O	Port A2	External Interrupt: EI0
46	34	PA3	I/O	Port A3	External Interrupt: EI0
47	35	V_{DD_1}	S	Main power supply	
48	36	V_{SS_1}	S	Ground	
49	37	PA4	I/O	Port A4	High Sink
50	38	PA5	I/O	Port A5	High Sink
51	39	PA6	I/O	Port A6	High Sink
52	40	PA7	I/O	Port A7	High Sink
53	41	TEST/V_{PP}[1)]	S	Test mode pin . In the EPROM programming mode, this pin acts as the programming voltage input V_{PP}.	This pin must be tied low in user mode
54	42	$\overline{\text{RESET}}$	I/O	Bidirectional. Active low. Top priority non maskable interrupt.	
55		NC		Not Connected	
56		NC		Not Connected	
57	43	V_{SS_2}	S	Ground	
58	44	OSCOUT	O	Input/Output Oscillator pin. These pins connect a parallel-resonant crystal, or an external source to the on-chip oscillator.	
59	45	OSCIN	I		
60	46	V_{DD_2}	S	Main power supply	
61	47	PE0/TDO	I/O	Port E1 or SCI Transmit Data Out	
62	48	PE1/RDI	I/O	Port E1 or SCI Receive Data In	
63		NC		Not Connected	
64		NC		Not Connected	

Note 1: V_{PP} on EPROM/OTP only.

Table 2. ST72331Jx Pin Description

Pin n° QFP44	Pin n° SDIP42	Pin Name	Type	Description	Remarks
1	38	PE1/RDI	I/O	Port E1 or SCI Receive Data In	
2	39	PB0	I/O	Port B0	External Interrupt: EI2
3	40	PB1	I/O	Port B1	External Interrupt: EI2
4	41	PB2	I/O	Port B2	External Interrupt: EI2
5	42	PB3	I/O	Port B3	External Interrupt: EI2
6	1	PB4	I/O	Port B4	External Interrupt: EI3
7	2	PD0/AIN0	I/O	Port D0 or ADC Analog Input 0	
8	3	PD1/AIN1	I/O	Port D1 or ADC Analog Input 1	
9	4	PD2/AIN2	I/O	Port D2 or ADC Analog Input 2	
10	5	PD3/AIN3	I/O	Port D3 or ADC Analog Input 3	
11	6	PD4/AIN4	I/O	Port D4 or ADC Analog Input 4	
12	7	PD5/AIN5	I/O	Port D5 or ADC Analog Input 5	
13	8	V_{DDA}	S	Power Supply for analog peripheral (ADC)	
14	9	V_{SSA}	S	Ground for analog peripheral (ADC)	
15	10	PF0/CLKOUT	I/O	Port F0 or CPU Clock Output	External Interrupt: EI1
16	11	PF1	I/O	Port F1	External Interrupt: EI1

Pin n° QFP44	Pin n° SDIP42	Pin Name	Type	Description	Remarks
17	12	PF2	I/O	Port F2	External Interrupt: EI1
18	13	PF4/OCMP1_A	I/O	Port F4 or Timer A Output Compare 1	
19	14	PF6/ICAP1_A	I/O	Port F6 or Timer A Input Capture 1	
20	15	PF7/EXTCLK_A	I/O	Port F7 or External Clock on Timer A	
21		V_{DD_0}	S	Main power supply	
22		V_{SS_0}	S	Ground	
23	16	PC0/OCMP2_B	I/O	Port C0 or Timer B Output Compare 2	
24	17	PC1/OCMP1_B	I/O	Port C1 or Timer B Output Compare 1	
25	18	PC2/ICAP2_B	I/O	Port C2 or Timer B Input Capture 2	
26	19	PC3/ICAP1_B	I/O	Port C3 or Timer B Input Capture 1	
27	20	PC4/MISO	I/O	Port C4 or SPI Master In / Slave Out Data	
28	21	PC5/MOSI	I/O	Port C5 or SPI Master Out / Slave In Data	
29	22	PC6/SCK	I/O	Port C6 or SPI Serial Clock	
30	23	PC7/$\overline{SS}$	I/O	Port C7 or SPI Slave Select	
31	24	PA3	I/O	Port A3	External Interrupt: EI0
32	25	V_{DD_1}	S	Main power supply	
33	26	V_{SS_1}	S	Ground	
34	27	PA4	I/O	Port A4	High Sink
35	28	PA5	I/O	Port A5	High Sink
36	29	PA6	I/O	Port A6	High Sink
37	30	PA7	I/O	Port A7	High Sink
38	31	TEST/V_{PP}[1)]	S	Test mode pin. In the EPROM programming mode, this pin acts as the programming voltage input V_{PP}.	This pin must be tied low in user mode
39	32	$\overline{RESET}$	I/O	Bidirectional. Active low. Top priority non maskable interrupt.	
40	33	V_{SS_2}	S	Ground	
41	34	OSCOUT	O	Input/Output Oscillator pin. These pins connect a parallel-resonant crystal, or an external source to the on-chip oscillator.	
42	35	OSCIN	I		
43	36	V_{DD_2}	S	Main power supply	
44	37	PE0/TDO	I/O	Port E0 or SCI Transmit Data Out	

Note 1: V_{PP} on EPROM/OTP only.

1.3 MEMORY MAP

Figure 6. Program Memory Map

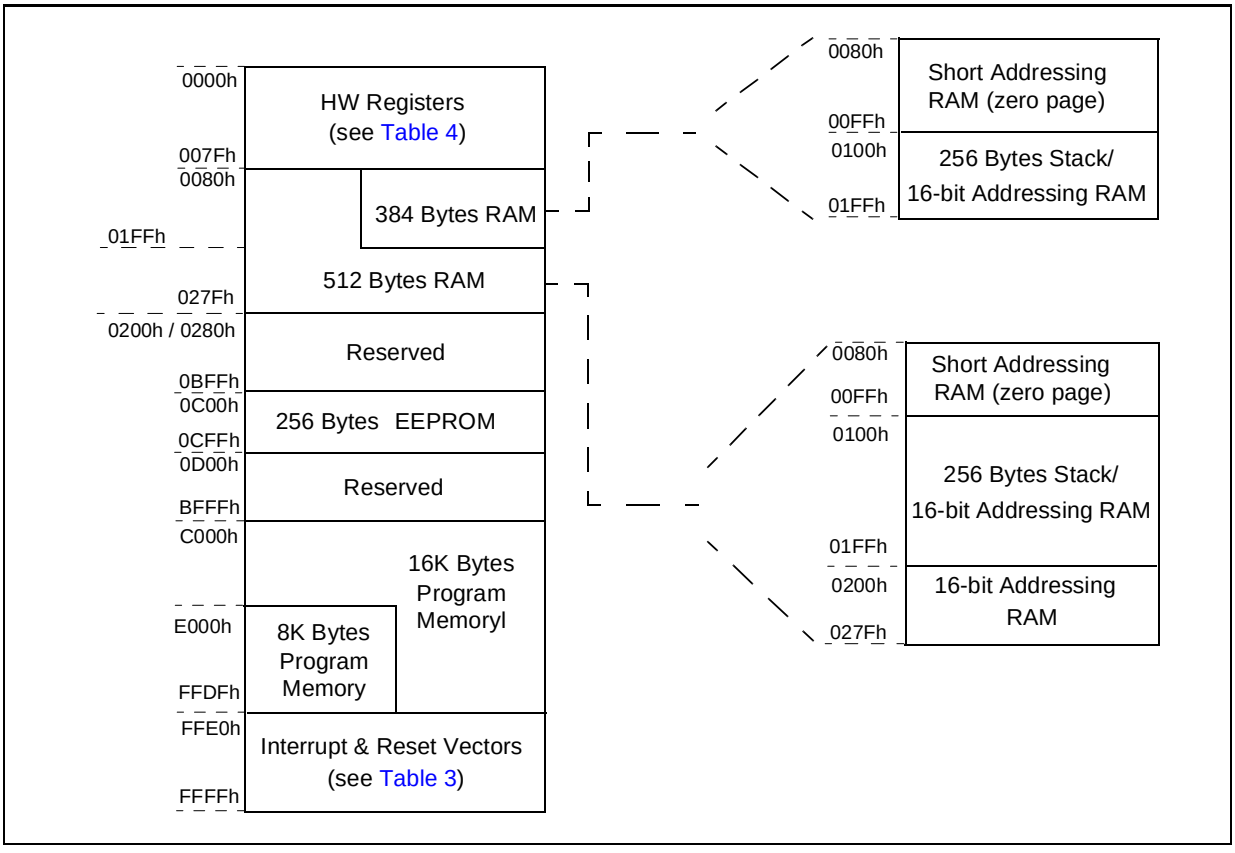


Table 3. Interrupt Vector Map

Vector Address	Description	Remarks
FFE0-FFE1h	Not Used	
FFE2-FFE3h	Not Used	
FFE4-FFE5h	EEPROM Interrupt Vector	Internal Interrupt
FFE6-FFE7h	SCI Interrupt Vector	Internal Interrupt
FFE8-FFE9h	TIMER B Interrupt Vector	Internal Interrupt
FFEA-FFEBh	TIMER A Interrupt Vector	Internal Interrupt
FFEC-FFEDh	SPI interrupt vector	Internal Interrupt
FFEE-FFEFh	Not Used	
FFF0-FFF1h	External Interrupt Vector EI3	External Interrupt
FFF2-FFF3h	External Interrupt Vector EI2	External Interrupt
FFF4-FFF5h	External Interrupt Vector EI1	External Interrupt
FFF6-FFF7h	External Interrupt Vector EI0	External Interrupt
FFF8-FFF9h	Not Used	
FFFA-FFFBh	Not Used	
FFFC-FFFDh	TRAP (software) Interrupt Vector	CPU Interrupt
FFFE-FFFFh	RESET Vector	

Table 4. Hardware Register Memory Map

Address	Block	Register Label	Register Name	Reset Status	Remarks
0000h	Port A	PADR	Data Register	00h	R/W
0001h		PADDR	Data Direction Register	00h	R/W
0002h		PAOR	Option Register	00h	R/W [1]
0003h	Reserved Area (1 byte)				
0004h	Port C	PCDR	Data Register	00h	R/W
0005h		PCDDR	Data Direction Register	00h	R/W
0006h		PCOR	Option Register	00h	R/W
0007h	Reserved Area (1 byte)				
0008h	Port B	PBDR	Data Register	00h	R/W
0009h		PBDDR	Data Direction Register	00h	R/W
000Ah		PBOR	Option Register	00h	R/W [1]
000Bh	Reserved Area (1 byte)				
000Ch	Port E	PEDR	Data Register	00h	R/W
000Dh		PEDDR	Data Direction Register	00h	R/W
000Eh		PEOR	Option Register	0Ch	R/W [1]
000Fh	Reserved Area (1 byte)				
0010h	Port D	PDDR	Data Register	00h	R/W
0011h		PDDDR	Data Direction Register	00h	R/W
0012h		PDOR	Option Register	00h	R/W [1]
0013h	Reserved Area (1 byte)				
0014h	Port F	PFDR	Data Register	00h	R/W
0015h		PFDDR	Data Direction Register	00h	R/W
0016h		PFOR	Option Register	28h	R/W [1]
0017h to 001Fh	Reserved Area (9 bytes)				
0020h		MISCR	Miscellaneous Register	00h	
0021h	SPI	SPIDR	SPI Data I/O Register	xxh	R/W
0022h		SPICR	SPI Control Register	xxh	R/W
0023h		SPISR	SPI Status Register	00h	Read Only
0024h to 0029h	Reserved Area (6 bytes)				
002Ah	WDG	WDGCR	Watchdog Control Register	7Fh	R/W
002Bh		WDGSR	Watchdog Status Register	00h	R/W [3]
002Ch	EEPROM	EEPCR	EEPROM Control Register	00h	R/W Register
002Dh to 0030h	Reserved Area (4 bytes)				

Address	Block	Register Label	Register Name	Reset Status	Remarks
0031h		TACR2	Control Register2	00h	R/W
0032h		TACR1	Control Register1	00h	R/W
0033h		TASR	Status Register	xxh	Read Only
0034h-0035h		TAIC1HR	Input Capture1 High Register	xxh	Read Only
		TAIC1LR	Input Capture1 Low Register	xxh	Read Only
0036h-0037h		TAOC1HR	Output Compare1 High Register	80h	R/W
		TAOC1LR	Output Compare1 Low Register	00h	R/W
0038h-0039h	Timer A	TACHR	Counter High Register	FFh	Read Only
		TACLR	Counter Low Register	FCh	Read Only
003Ah-003Bh		TAACHR	Alternate Counter High Register	FFh	Read Only
		TAACLR	Alternate Counter Low Register	FCh	Read Only
003Ch-003Dh		TAIC2HR	Input Capture2 High Register	xxh	Read Only[2]
		TAIC2LR	Input Capture2 Low Register	xxh	Read Only[2]
003Eh-003Fh		TAOC2HR	Output Compare2 High Register	80h	R/W[2]
		TAOC2LR	Output Compare2 Low Register	00h	R/W[2]
0040h	Reserved Area (1 byte)				
0041h		TBCR2	Control Register2	00h	R/W
0042h		TBCR1	Control Register1	00h	R/W
0043h		TBSR	Status Register	xxh	Read Only
0044h-0045h		TBIC1HR	Input Capture1 High Register	xxh	Read Only
		TBIC1LR	Input Capture1 Low Register	xxh	Read Only
0046h-0047h		TBOC1HR	Output Compare1 High Register	80h	R/W
		TBOC1LR	Output Compare1 Low Register	00h	R/W
0048h-0049h	Timer B	TBCHR	Counter High Register	FFh	Read Only
		TBCLR	Counter Low Register	FCh	Read Only
004Ah-004Bh		TBACHR	Alternate Counter High Register	FFh	Read Only
		TBACLR	Alternate Counter Low Register	FCh	Read Only
004Ch-004Dh		TBIC2HR	Input Capture2 High Register	xxh	Read Only
		TBIC2LR	Input Capture2 Low Register	xxh	Read Only
004Eh-004Fh		TBOC2HR	Output Compare2 High Register	80h	R/W
		TBOC2LR	Output Compare2 Low Register	00h	R/W
0050h		SCISR	SCI Status Register	C0h	Read Only
0051h		SCIDR	SCI Data Register	xxh	R/W
0052h		SCIBRR	SCI Baud Rate Register	00x----xb	R/W
0053h	SCI	SCICR1	SCI Control Register 1	xxh	R/W
0054h		SCICR2	SCI Control Register 2	00h	R/W
0055h		SCIERPR	SCI Extended Receive Prescaler Register	00h	R/W
0056h			Reserved	---	Reserved
0057h		SCIETPR	SCI Extended Transmit Prescaler Register	00h	R/W
0058h to 006Fh	Reserved Area (24 bytes)				
0070h	ADC	ADCDR	ADC Data Register	00h	Read Only
0071h		ADCCSR	ADC Control/Status Register	00h	R/W
0072h to 007Fh	Reserved Area (14 bytes)				

Notes:
1. The bits corresponding to unavailable pins are forced to 1 by hardware, this affects the reset status value.
2. External pin not available.
3. Not used in versions without Low Voltage Detector Reset.

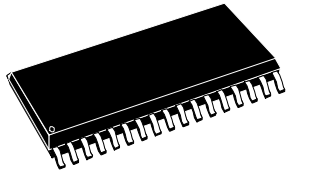
Notes:

ST72272

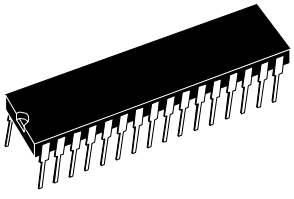
8-BIT MCUs WITH 8 TO 16K ROM/OTP/EPROM, 384 TO 512 BYTES RAM, ADC, DAC (PWM), TIMER AND I^2C

PRELIMINARY DATA

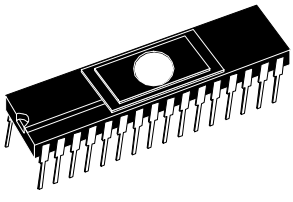
- User Program Memory ROM/OTP/EPROM: 8 to 16K bytes
- Data RAM: 384 to 512 bytes (256 bytes stack)
- Master Reset and Power-On Reset
- Run, Wait, Slow, Halt and RAM Retention modes
- 18 I/O lines:
  - 1 programmable interrupt input
  - 5 high sink outputs
  - 4 analog alternate inputs
  - 8 alternate functions
  - EMI filtering
- Programmable watchdog (WDG)
- 16-bit Timer with 2 Input Capture and 2 Output Compare functions (with 1 output pin)
- 8-bit Analog to Digital Converter with 4 channels
- Four 10-bit Digital to Analog Converter channels with PWM output
- Fast I^2C Multi Master Interface
- 63 basic instructions and 17 main address modes
- 8x8 unsigned multiply instruction
- True bit manipulation
- Versatile Development Tools (DOS and Windows) including assembler, linker, C-compiler, archiver, source level debugger, and hardware emulator



PSO34



PSDIP32



CSDIP32

Device Summary

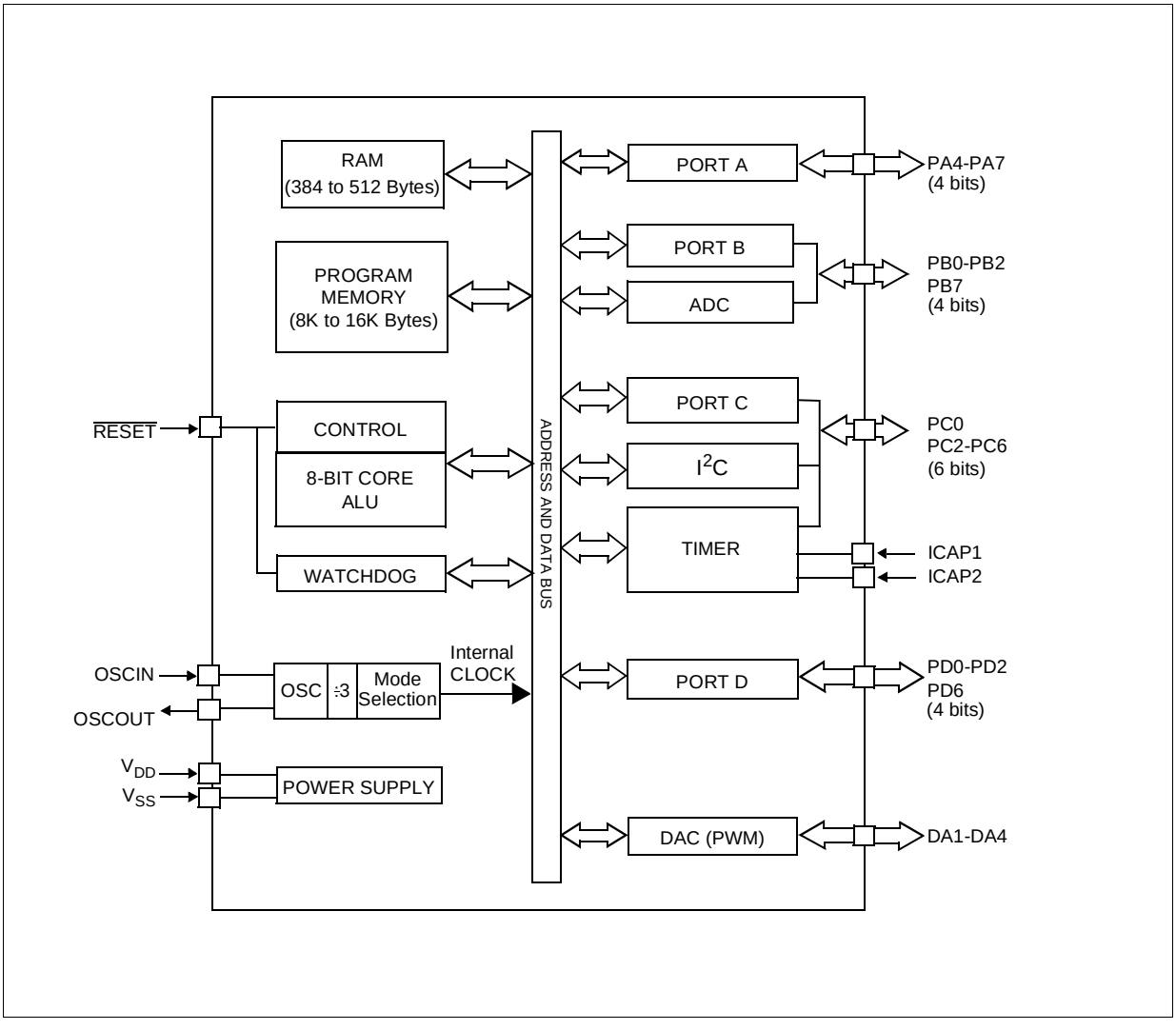
Features	ST72272K2	ST72272K4
Program Memory - bytes	8K	16K
RAM (stack) - bytes	384 (256)	512 (256)
10-Bit D/A Converter	4 channels	
A/D Converter	4 channels	
16-Bit Timer	1	
I^2C Bus	1 multimaster	
I/Os	24	
Operating Supply	4.0 to 5.5 V	
CPU Frequency	8 MHz max (24 MHz quartz)	
Temperature Range	0°C to + 70°C	
Package	SO34 - SDIP32	

1 GENERAL DESCRIPTION

1.1 INTRODUCTION

The ST72272 series is a HCMOS microcontroller unit (MCU) from the ST7 family with a dedicated D/A Converter peripherals offering 4 PWM outputs.
It is based around an industry standard 8-bit core and offers an enhanced instruction set. The processor runs with an external clock up to 24 MHz with a 5.5V supply. Due to the fully static design of this device, operation down to DC is possible. Under software control the ST72272 can be placed in WAIT, SLOW or HALT mode thus reducing power consumption. The enhanced instruction set and addressing modes afford real programming potential.
In addition to standard 8-bit data management the ST7 features true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes on the whole memory.
The device includes an on-chip oscillator, CPU, 8 to 16 Kbytes ROM/OTP/EPROM, 384 to 512 bytes RAM, 18 I/O lines, a Timer with 2 Input Captures and 2 Output Compares, a 4-channel A/D Converter, an I^2C multi Master, a Watchdog Reset and a 4-channel 10-bit D/A Converter with PWM output.

Figure 1. ST72272 Block Diagram



1.2 PIN DESCRIPTION

Figure 2. 34-Pin SO Package Pinout

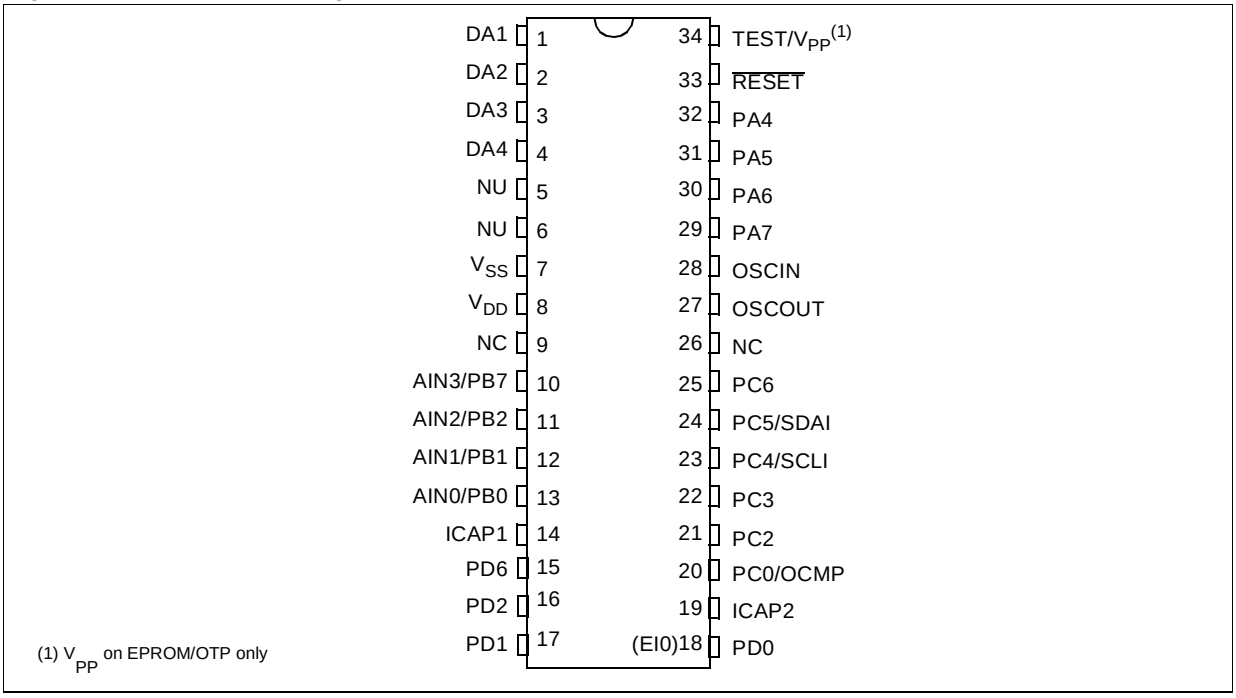
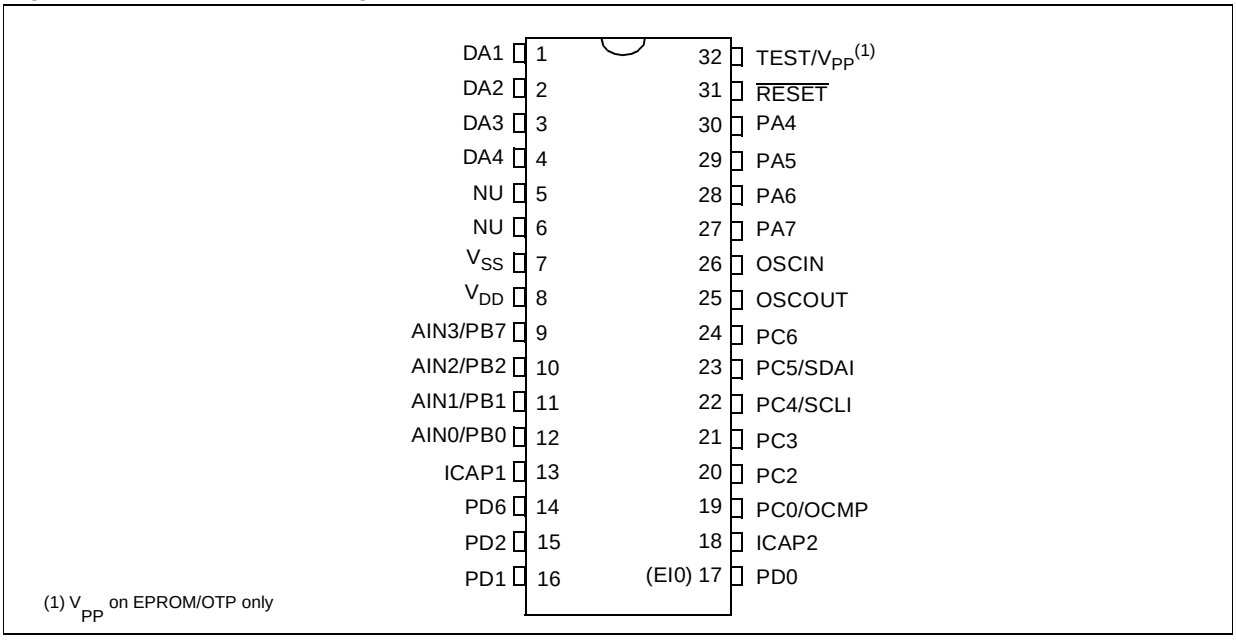


Figure 3. 32-Pin SDIP Package Pinout



Note: Several pins of the I/O ports assume software programmable alternate functions as shown in the pin description.

PIN DESCRIPTION (Cont'd)

Table 1. 34-Pin SO and 32-Pin SDIP Package Pin Description

Pin n° SO34	Pin n° SDIP32	Pin Name	Type	Description	Remarks
1	1	DA1	O	10-bit D/A (PWM output)	For analog controls, after external filtering
2	2	DA2	O	10-bit D/A (PWM output)	
3	3	DA3	O	10-bit D/A (PWM output)	
4	4	DA4	O	10-bit D/A (PWM output)	
5	5	NU		Non User pin. Must be left unconnected	
6	6	NU		Non User pin. Must be left unconnected	
7	7	V_{SS}	S	Ground	
8	8	V_{DD}	S	Main power supply	
9		NC		Not Connected	
10	9	PB7/AIN3	I/O	Port B7 or ADC Analog Input 3	
11	10	PB2/AIN2	I/O	Port B6 or ADC Analog Input 2	
12	11	PB1/AIN1	I/O	Port B5 or ADC Analog Input 1	
13	12	PB0/AIN0	I/O	Port B4 or ADC Analog Input 0	
14	13	ICAP1		Timer Input Capture 1	Not for general purpose I/O
15	14	PD6	I/O	Port D6	
16	15	PD2	I/O	Port D2	
17	16	PD1	I/O	Port D1	
18	17	PD0	I/O	Port D0	External Interrupt: EI0
19	18	ICAP2		Timer Input Capture 2 with 256 prescaler	Not for general purpose I/O
20	19	PC0/OCMP	I/O	Port C0 or Timer Output Compare	
21	20	PC2	I/O	Port C2	
22	21	PC3	I/O	Port C3	
23	22	PC4/SCLI	I/O	Port C4 or I^2C Serial Clock	
24	23	PC5/SDAI	I/O	Port C5 or I^2C Serial Data	
25	24	PC6	I/O	Port C6	High Current
26		NC		Not Connected	
27	25	OSCOUT	O	Input/Output Oscillator pin. These pins connect a parallel-resonant crystal, or an external source to the on-chip oscillator.	
28	26	OSCIN	I		
29	27	PA7	I/O	Port A7	High Current
30	28	PA6	I/O	Port A6	High Current
31	29	PA5	I/O	Port A5	High Current
32	30	PA4	I/O	Port A4	High Current
33	31	$\overline{\text{RESET}}$	I/O	Bidirectional. Active low. Top priority non maskable interrupt.	It can be used to reset external peripherals.
34	32	V_{PP}/TEST	S	Test mode pin. In EPROM devices acts as programming voltage input V_{PP}.	This pin should be tied low in user mode

Note: S= Supply

1.3 MEMORY MAP

Figure 4. Program Memory Map

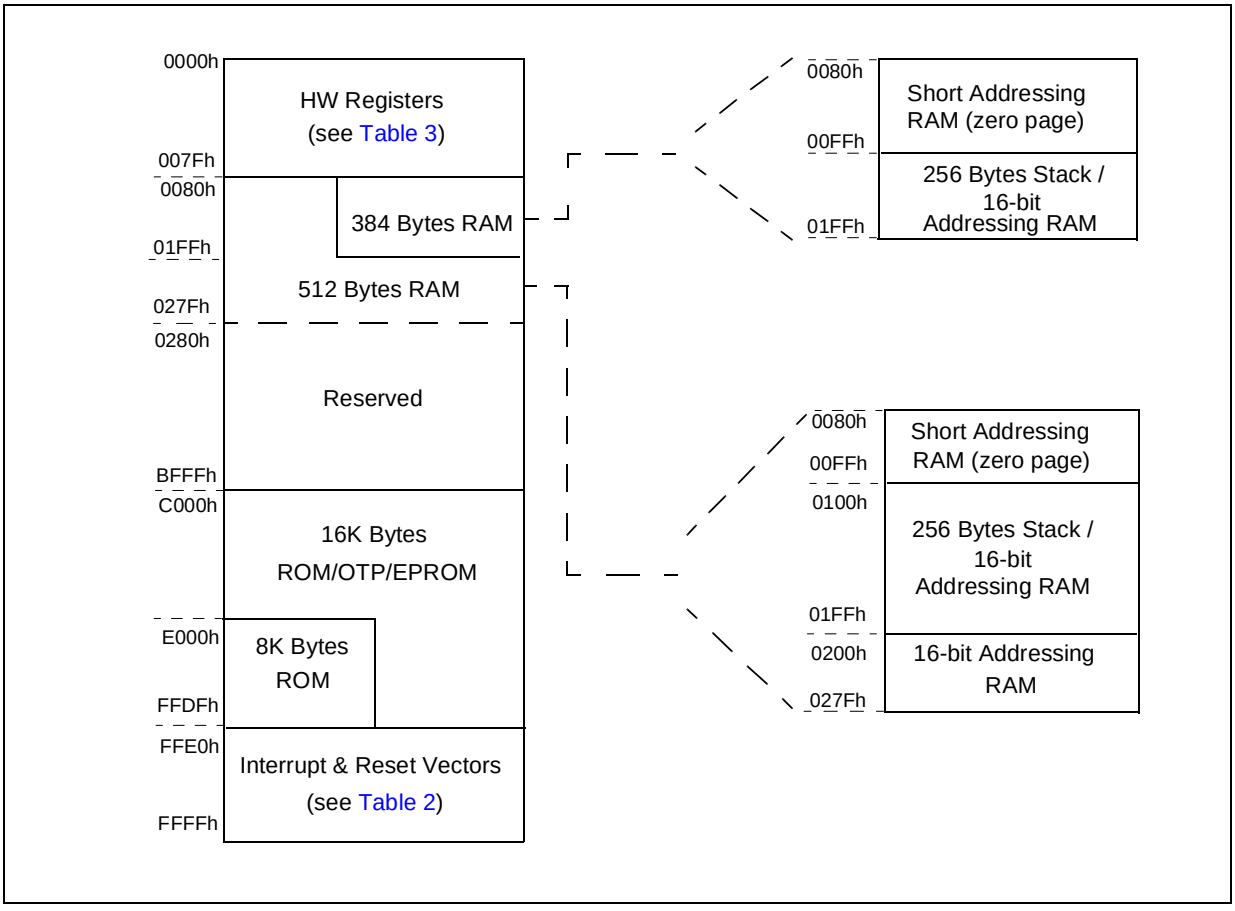


Table 2. Interrupt Vector Map

Vector Address	Description	Remarks
FFE0-FFE1h	Reserved	
FFE2-FFE3h	Reserved	
FFE4-FFE5h	I^2C Interrupt Vector	Internal Interrupts
FFE6-FFE7h	Timer Overflow Interrupt Vector	“
FFE8-FFE9h	Timer Output Compare Interrupt Vector	“
FFEA-FFEBh	Timer Input Capture Interrupt Vector	“
FFEC-FFEDh	Reserved	
FFEE-FFEFh	Reserved	
FFF0-FFF1h	EI0 Interrupt Vector	External Interrupt
FFF2-FFF3h	Reserved	
FFF4-FFF5h	Reserved	
FFF6-FFF7h	Reserved	
FFF8-FFF9h	Reserved	
FFFA-FFFBh	Reserved	
FFFC-FFFDh	TRAP Interrupt Vector	Software Interrupt
FFFE-FFFFh	RESET Vector	CPU Interrupt

MEMORY MAP (Cont'd)

Table 3. Hardware Register Memory Map

Address	Block	Register Label	Register Name	Reset Status	Remarks
0000h 0001h	Port A	PADR PADDR	Port A Data Register Port A Data Direction Register	00h 00h	R/W R/W
0002h 0003h	Port C	PCDR PCDDR	Port C Data Register Port C Data Direction Register	00h 00h	R/W R/W
0004h 0005h	Port D	PDDR PDDDR	Port D Data Register Port D Data Direction Register	00h 00h	R/W R/W
0006h 0007h 0008h	Port B	PBDR PBDDR PBICFGR	Port B Data Register Port B Data Direction Register Port B Input Pull-Up Configuration Register	00h 00h 00h	R/W R/W R/W
0009h		MISCR	Miscellaneous Register	00h	R/W
000Ah 000Bh	ADC	ADCDR ADCCSR	ADC Data Register ADC Control Status register	00h 00h	Read only R/W
000Ch	WDG	WDGCR	Watchdog Control Register	7Fh	R/W
000Dh 000Fh	Reserved Area (3 bytes)				
00010h	ITR	ITRFRE	Interrupt Register	00h	R/W
0011h 0012h 0013h 0014h 0015h 0016h 0017h 0018h 0019h 001Ah 001Bh 001Ch 001Dh 001Eh 001Fh	TIM	TIMCR2 TIMCR1 TIMSR TIMIC1HR TIMIC1LR TIMOC1HR TIMOC1LR TIMCHR TIMCLR TIMACHR TIMACLR TIMIC2HR TIMIC2LR TIMOC2HR TIMOC2LR	Timer Control Register 2 Timer Control Register 1 Timer Status Register Timer Input Capture 1 High Register Timer Input Capture 1 Low Register Timer Output Compare 1 High Register Timer Output Compare 1 Low Register Timer Counter High Register Timer Counter Low Register Timer Alternate Counter High Register Timer Alternate Counter Low Register Timer Input Capture 2 High Register Timer Input Capture 2 Low Register Timer Output Compare 2 High Register Timer Output Compare 2 Low Register	00h 00h 00h xxh xxh 80h 00h FFh FCh FFh FCh xxh xxh 80h 00h	R/W R/W Read only Read only Read only R/W R/W Read only Read only Read only Read only Read only Read only R/W R/W
0020h 0023h	Reserved Area (4 bytes)				
0024h 0025h 0026h 0027h 0028h 0029h		PWM1 BRM21 PWM2 PWM3 BRM43 PWM4	10 BIT PWM / BRM Register	80h 00h 80h 80h 00h 80h	R/W R/W R/W R/W R/W R/W
002Ah to 0042h	Reserved Area (25 bytes)				
0043h	TIM		ICAP Pin Configuration **Warning:** Write 0Ch in this register to use the ICAP1 and ICAP2 functions.	08h	R/W

Address	Block	Register Label	Register Name	Reset Status	Remarks
0044h 0058h	Reserved Area (21 bytes)				
0059h 005Ah 005Bh 005Ch 005Dh 005Eh 005Fh	I^2C	I2CDR I2COAR I2CCCR I2CSR2 I2CSR1 I2CCR	I^2C Data Register Reserved I^2C (7 Bits) Slave Address Register I^2C Clock Control Register I^2C Status Register 2 I^2C Status Register 1 I^2C Control Register	00h 00h 00h 00h 00h 00h	R/W R/W R/W Read only Read only R/W
0060h to 007Fh	Reserved Area (32 bytes)				

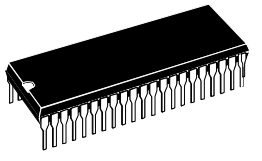
Notes

ST72371/ST72372

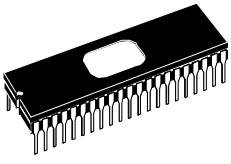
8-BIT MCUs WITH 16K ROM/OTP/EPROM, 512 BYTES RAM, ADC, DAC (PWM), TIMER, I²C AND SCI

PRELIMINARY DATA

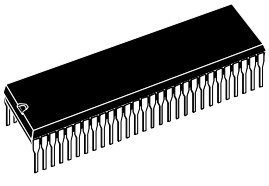
- User Program Memory (ROM/OTP/EPROM): 16K bytes
- Data RAM: 512 bytes, including 256 bytes of stack
- Master Reset and Power-On Reset
- Run, Wait, Slow, Halt and RAM Retention modes
- 23 to 32 I/O lines:
  - 4 to 5 programmable interrupt inputs
  - 6 to 8 high sink outputs
  - 4 to 8 analog alternate inputs
  - 10 to 14 alternate functions
  - EMI filtering
- Programmable watchdog (WDG)
- 16-bit Timer, featuring:
  - 2 Input Captures
  - 2 Output Compares (with 1 output pin)
  - PWM and Pulse Generator modes
- 8-bit Analog-to-Digital converter (4 to 8 channels)
- Four 10-bit and one 12-bit Digital to Analog Converter Channels with PWM output
- Fast I²C Multimaster Interface
- Serial Communications Interface (SCI) (ST72371N only)
- 8-bit Data Manipulation
- 63 Basic Instructions
- 17 main Addressing Modes
- 8 x 8 Unsigned Multiply Instruction
- True Bit Manipulation
- Complete Development Support on PC/DOS-WINDOWS™ Real-Time Emulator
- Full Software Package on DOS/WINDOWS™ (C-Compiler, Cross-Assembler, Debugger)



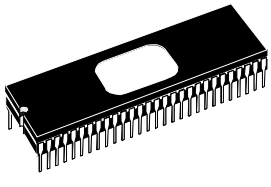
PSDIP42



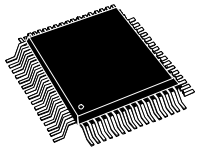
CSDIP42W



PSDIP56



CSDIP56



TQFP64

Device Summary

Features	ST72372J4	ST72371N4
Program Memory - bytes	16K	
RAM (stack) - bytes	512 (256)	
10-Bit D/A Converter	4 channels	
12-Bit D/A Converter	1 channel	
A/D Converter	4 channels	8 channels
16-Bit Timer	1	
I²C Bus	1 multimaster	
SCI	No	Yes
I/Os	30	39
Operating Supply	4.0 to 5.5 V	
CPU Frequency	8 MHz max (24 MHz quartz)	
Temperature Range	0°C to + 70°C	
Package	SDIP42	SDIP56-TQFP64

1 GENERAL DESCRIPTION

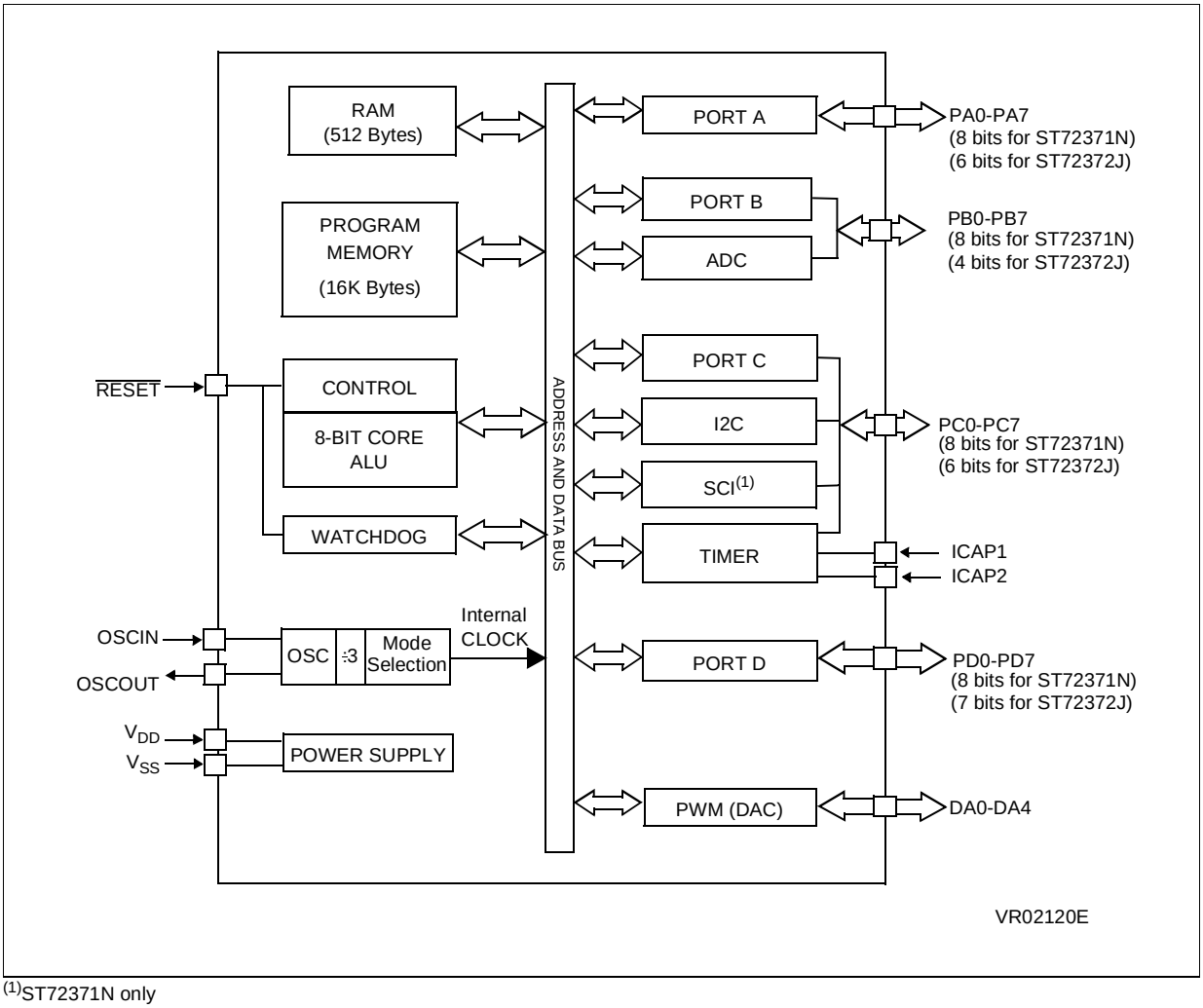
1.1 INTRODUCTION

The ST72371/ST72372 HCMOS Microcontroller Units are members of the ST7 family. These devices are based on an industry standard 8-bit core and feature an enhanced instruction set. The processor runs with an external clock up to 24 MHz with a 5.5V supply. Under software control the ST72371/ST72372 can be placed in WAIT, SLOW or HALT modes thus reducing power consumption. The enhanced instruction set and addressing modes afford real programming potential.

In addition to standard 8-bit data management the ST7 features true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes on the whole memory.

The devices include an on-chip oscillator, CPU, 16K bytes program memory, 512 bytes RAM, 23 to 32 I/O lines, a Timer with 2 Input Captures and 2 Output Compares (with 1 output pin), a 4 to 8 channel A/D Converter, an I^2C multi Master, an SCI(1) Serial Communications Interface, a Watchdog Reset, four 10-bit and one 12-bit D/A Converter channels with PWM output.

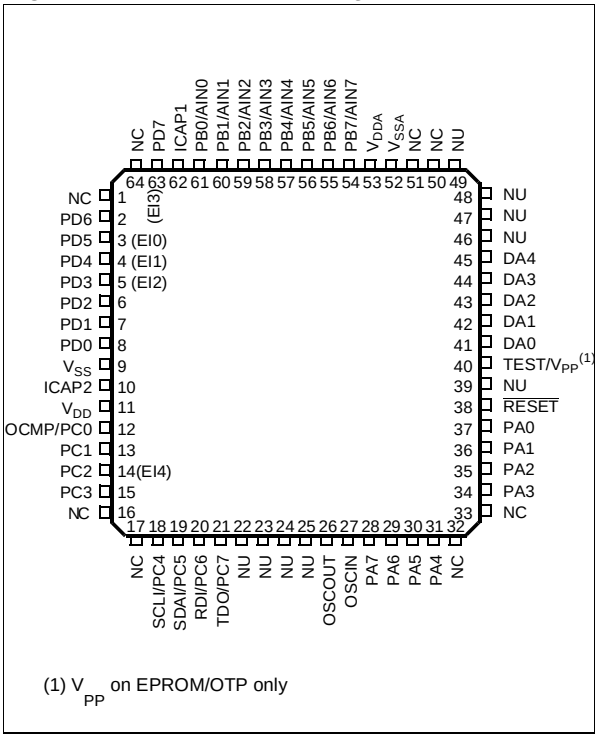
Figure 1. ST72371/ST72372 Block Diagram



(1)ST72371N only

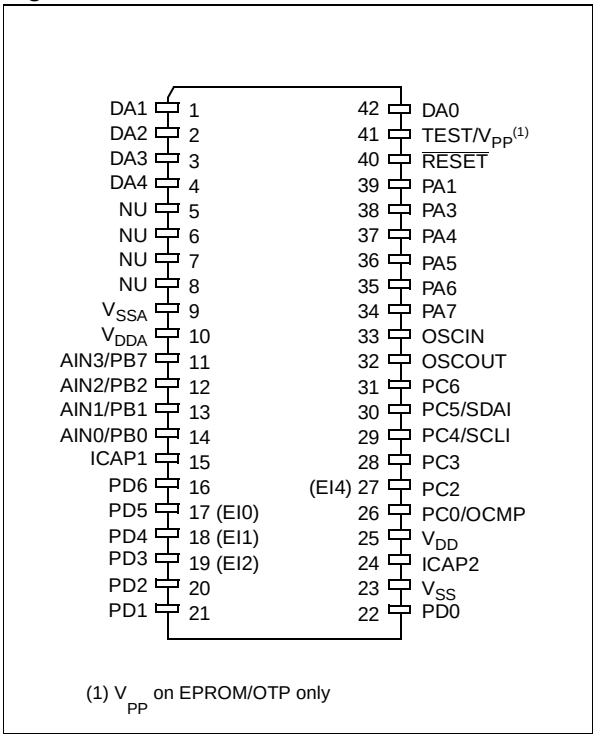
1.2 PIN DESCRIPTION

Figure 2. ST72371N 64-Pin QFP Pinout



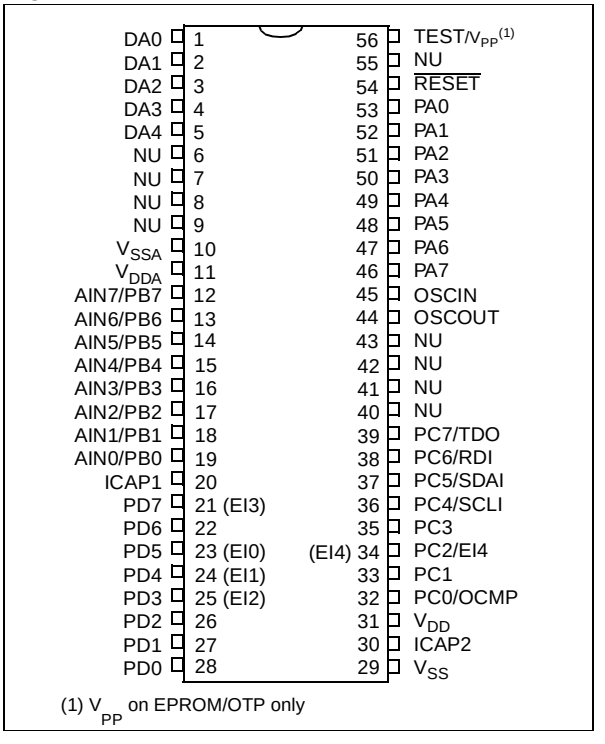
(1) V_{PP} on EPROM/OTP only

Figure 3. ST72371J 42-Pin SDIP Pinout



(1) V_{PP} on EPROM/OTP only

Figure 4. ST72371N 56-Pin SDIP Pinout



(1) V_{PP} on EPROM/OTP only

Note: Several pins of the I/O ports assume software programmable alternate functions as shown in the pin description.

PIN DESCRIPTION (Cont'd)

Table 1. ST72371N Pin Description

Pin n° QFP64	Pin n° SDIP56	Pin Name	Type	Description	Remarks
1		NC		Not Connected	
2	22	PD6	I/O	Port D6	
3	23	PD5	I/O	Port D5	External Interrupt: EI0
4	24	PD4	I/O	Port D4	External Interrupt: EI1
5	25	PD3	I/O	Port D3	External Interrupt: EI2
6	26	PD2	I/O	Port D2	
7	27	PD1	I/O	Port D1	
8	28	PD0	I/O	Port D0	
9	29	V_{SS}	S	Ground	
10	30	ICAP2	I	Timer Input Capture 2 with 256 prescaler	Not for general purpose I/O
11	31	V_{DD}	S	Main power supply	
12	32	PC0/OCMP	I/O	Port C0 or Timer Output Compare	
13	33	PC1	I/O	Port C1	
14	34	PC2	I/O	Port C2	External Interrupt: EI4
15	35	PC3	I/O	Port C3	
16		NC		Not Connected	
17		NC		Not Connected	
18	36	PC4/SCLI	I/O	Port C4 or I^2C Serial Clock	
19	37	PC5/SDAI	I/O	Port C5 or I^2C Serial Data	
20	38	PC6/RDI	I/O	Port C6, or SCI Receive Data Input	
21	39	PC7/TDO	I/O	Port C7 or SCI Transmit Data Output	
22	40	NU		Non User pin. Must be left unconnected	
23	41	NU		Non User pin. Must be left unconnected	
24	42	NU		Non User pin. Must be left unconnected	
25	43	NU		Non User pin. Must be left unconnected	
26	44	OSCOUT	O	Input/Output Oscillator pin.These pins connect a parallel-resonant crystal, or an external source to the on-chip oscillator.	
27	45	OSCIN	I		
28	46	PA7	I/O	Port A7, High Sink	
29	47	PA6	I/O	Port A6, High Sink	
30	48	PA5	I/O	Port A5, High Sink	
31	49	PA4	I/O	Port A4, High Sink	
32		NC		Not Connected	
33		NC		Not Connected	
34	50	PA3	I/O	Port A3, High Sink	
35	51	PA2	I/O	Port A2, High Sink	
36	52	PA1	I/O	Port A1, High Sink	
37	53	PA0	I/O	Port A0, High Sink	
38	54	$\overline{\text{RESET}}$	I/O	Bidirectional. Active low. Top priority non maskable interrupt.	Can be used to reset external peripherals.
39	55	NU	I/O	Non User pin. Must be left unconnected	

Pin n° QFP64	Pin n° SDIP56	Pin Name	Type	Description	Remarks
40	56	TEST/V_{PP}	S	Test mode pin. In EPROM devices acts as programming voltage input V_{PP}.	This pin should be tied low in user mode
41	1	DA0	O	12-bit D/A (PWM output)	For analog controls, after external filtering
42	2	DA1	O	10-bit D/A (PWM output)	
43	3	DA2	O	10-bit D/A (PWM output)	
44	4	DA3	O	10-bit D/A (PWM output)	
45	5	DA4	O	10-bit D/A (PWM output)	
46	6	NU		Non User pin. Must be left unconnected	
47	7	NU		Non User pin. Must be left unconnected	
48	8	NU		Non User pin. Must be left unconnected	
49	9	NU		Non User pin. Must be left unconnected	
50		NC		Not Connected	
51		NC		Not Connected	
52	10	V_{SSA}	S	Ground for analog peripheral (ADC)	Must be connected externally to V_{ss}
53	11	V_{DDA}	S	Power Supply for analog peripheral (ADC)	Must be connected externally to V_{DD}
54	12	PB7/AIN7	I/O	Port B7 or ADC analog input 7	
55	13	PB6/AIN6	I/O	Port B6 or ADC analog input 6	
56	14	PB5/AIN5	I/O	Port B5 or ADC analog input 5	
57	15	PB4/AIN4	I/O	Port B4 or ADC analog input 4	
58	16	PB3/AIN3	I/O	Port B3 or ADC analog input 3	
59	17	PB2/AIN2	I/O	Port B2 or ADC analog input 2	
60	18	PB1/AIN1	I/O	Port B1 or ADC analog input 1	
61	19	PB0/AIN0	I/O	Port B0 or ADC analog input 0	
62	20	ICAP1	I	Timer Input Capture 1	Not for general purpose I/O
63	21	PD7	I/O	Port D7	External Interrupt: EI3
64		NC		Not Connected	

Table 2. ST72372J Pin Description

Pin	Pin Name	Type	Description	Remarks
1	DA1	O	10-bit D/A (PWM output)	For analog controls, after external filtering
2	DA2	O	10-bit D/A (PWM output)	
3	DA3	O	10-bit D/A (PWM output)	
4	DA4	O	10-bit D/A (PWM output)	
5	NU		Non User pin. Must be left unconnected	
6	NU		Non User pin. Must be left unconnected	
7	NU		Non User pin. Must be left unconnected	
8	NU		Non User pin. Must be left unconnected	
9	V_{SSA}	S	Ground for analog peripheral (ADC)	Must be connected externally to V_{ss}
10	V_{DDA}	S	Power Supply for analog peripheral (ADC)	Must be connected externally to V_{DD}
11	PB7/AIN3	I/O	Port B7 or ADC analog input 3	
12	PB2/AIN2	I/O	Port B2 or ADC analog input 2	

Pin	Pin Name	Type	Description	Remarks
13	PB1/AIN1	I/O	Port B1 or ADC analog input 1	
14	PB0/AIN0	I/O	Port B0 or ADC analog input 0	
15	ICAP1	I	Timer Input Capture 1	Not for general purpose I/O
16	PD6	I/O	Port D6	
17	PD5	I/O	Port D5	External Interrupt: EI0
18	PD4	I/O	Port D4	External Interrupt: EI1
19	PD3	I/O	Port D3	External Interrupt: EI2
20	PD2	I/O	Port D2	
21	PD1	I/O	Port D1	
22	PD0	I/O	Port D0	
23	V_{SS}	S	Ground	
24	ICAP2	I	Timer Input Capture 2 with 256 prescaler	Not for general purpose I/O
25	V_{DD}	S	Main power supply	
26	PC0/OCMP	I/O	Port C0 or Timer Output Compare	
27	PC2	I/O	Port C2	External Interrupt: EI4
28	PC3	I/O	Port C3	
29	PC4/SCLI	I/O	Port C4 or I^2C Serial Clock	
30	PC5/SDAI	I/O	Port C5 or I^2C Serial Data	
31	PC6	I/O	Port C6, High Sink	
32	OSCOUT	O	Input/Output Oscillator pin. These pins connect a parallel-resonant crystal, or an external source to the on-chip oscillator.	
33	OSCIN	I		
34	PA7	I/O	Port A7, High Sink	
35	PA6	I/O	Port A6, High Sink	
36	PA5	I/O	Port A5, High Sink	
37	PA4	I/O	Port A4, High Sink	
38	PA3	I/O	Port A3, High Sink	
39	PA1	I/O	Port A1, High Sink	
40	$\overline{\text{RESET}}$	I/O	Bidirectional. Active low signal. Top priority non maskable interrupt.	Can be used to reset external peripherals.
41	TEST/V_{PP}	S	Test mode pin or EPROM programming voltage. In EPROM devices acts as programming voltage input V_{PP}.	This pin should be tied low in user mode
42	DA0	O	12-bit DAC (PWM output)	For analog controls, after external filtering

Note: S= Supply

1.3 MEMORY MAP

Figure 5. Program Memory Map

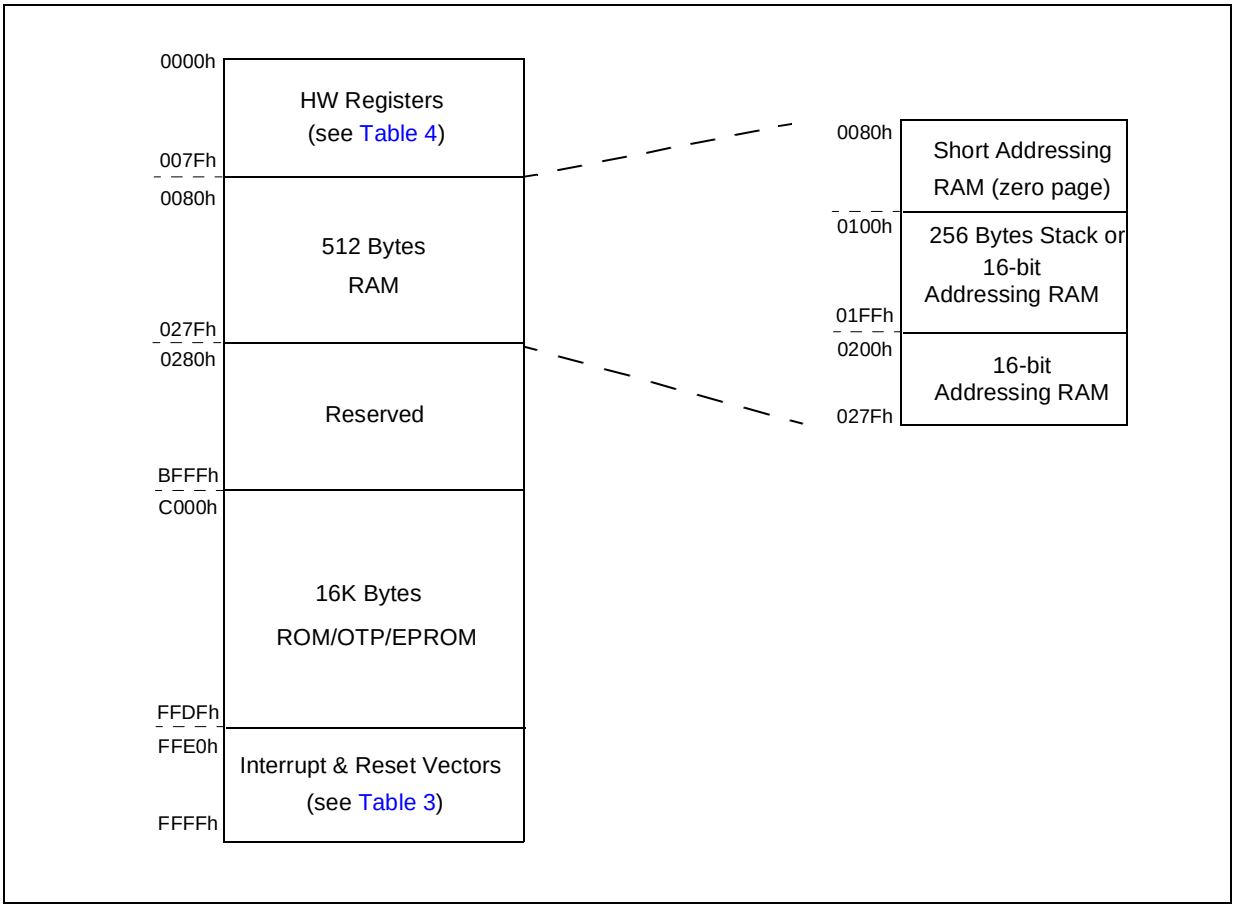


Table 3. Interrupt Vector Map

Vector Address	Description	Remarks
FFE0-FFE1h	Reserved	
FFE2-FFE3h	SCI Interrupt Vector	Internal Interrupts
FFE4-FFE5h	I^2C Interrupt Vector	“
FFE6-FFE7h	Timer Overflow Interrupt Vector	“
FFE8-FFE9h	Timer Output Compare Interrupt Vector	“
FFEA-FFEBh	Timer Input Capture Interrupt Vector	“
FFEC-FFEDh	Reserved	
FFEE-FFEFh	EI4 Interrupt Vector	External Interrupts
FFF0-FFF1h	EI0 Interrupt Vector	“
FFF2-FFF3h	EI1 Interrupt Vector	“
FFF4-FFF5h	EI2 Interrupt Vector	“
FFF6-FFF7h	EI3 Interrupt Vector	“
FFF8-FFF9h	Reserved	
FFFA-FFFBh	Reserved	
FFFC-FFFDh	TRAP Interrupt Vector	Software Interrupt
FFFE-FFFFh	RESET Vector	CPU Interrupt

MEMORY MAP (Cont'd)

Table 4. Hardware Register Memory Map

Address	Block	Register Label	Register Name	Reset Status	Remarks
0000h 0001h	Port A	PADR PADDR	Port A Data Register Port A Data Direction Register	00h 00h	R/W R/W
0002h 0003h	Port C	PCDR PCDDR	Port C Data Register Port C Data Direction Register	00h 00h	R/W R/W
0004h 0005h	Port D	PDDR PDDDR	Port D Data Register Port D Data Direction Register	00h 00h	R/W R/W
0006h 0007h 0008h	Port B	PBDR PBDDR PBOR	Port B Data Register Port B Data Direction Register Port B Option Register	00h 00h 00h	R/W R/W R/W
0009h		MISCR	Miscellaneous Register	00h	R/W
000Ah 000Bh	ADC	ADCDR ADCCSR	ADC Data Register ADC Control Status register	00h 00h	Read only R/W
000Ch	WDG	WDGCR	Watchdog Control Register	7Fh	R/W
000Dh 000Fh	Reserved Area (3 bytes)				
0010h	ITR	ITRFRE	Interrupt Register	00h	R/W
0011h 0012h 0013h 0014h 0015h 0016h 0017h 0018h 0019h 001Ah 001Bh 001Ch 001Dh 001Eh 001Fh	TIM	TIMCR2 TIMCR1 TIMSR TIMIC1HR TIMIC1LR TIMOC1HR TIMOC1LR TIMCHR TIMCLR TIMACHR TIMACLR TIMIC2HR TIMIC2LR TIMOC2HR TIMOC2LR	Timer Control Register 2 Timer Control Register 1 Timer Status Register Timer Input Capture 1 High Register Timer Input Capture 1 Low Register Timer Output Compare 1 High Register Timer Output Compare 1 Low Register Timer Counter High Register Timer Counter Low Register Timer Alternate Counter High Register Timer Alternate Counter Low Register Timer Input Capture 2 High Register Timer Input Capture 2 Low Register Timer Output Compare 2 High Register Timer Output Compare 2 Low Register	00h 00h 00h xxh xxh 80h 00h FFh FCh FFh FCh xxh xxh 80h 00h	R/W R/W Read only Read only Read only R/W R/W Read only Read only Read only Read only Read only Read only R/W R/W
0020h 0021h	Reserved Area (2 bytes)				
0022h 0023h	DAC	PWM0 BRM0	12-BIT PWM Register 12-BIT BRM Register	80h C0h	R/W R/W
0024h 0025h 0026h 0027h 0028h 0029h		PWM1 BRM21 PWM2 PWM3 BRM43 PWM4	10-BIT PWM / BRM Registers	80h 00h 80h 80h 00h 80h	R/W R/W R/W R/W R/W R/W
002Ah to 002Fh	Reserved Area (6 bytes)				

Address	Block	Register Label	Register Name	Reset Status	Remarks
0030h 0031h 0032h 0033h 0034h	SCI	SCISR SCIDR SCIBRR SCICR1 SCICR2	SCI Status Register SCI Data Register SCI Baud Rate Register SCI Control Register 1 SCI Control Register 2	C0h xxh 00xx xxxxb xxh 00h	Read only R/W R/W R/W R/W
0035h to 0042h	Reserved Area (14 bytes)				
0043h	TIM	CONFIG	ICAP Pin Configuration **Warning:** Write 0Ch in this register to use the ICAP1 and ICAP2 functions.	08h	R/W
0044h to 0058h	Reserved Area (21 bytes)				
0059h 005Ah 005Bh 005Ch 005Dh 005Eh 005Fh	I^2C	I2CDR I2COAR I2CCCR I2CSR2 I2CSR1 I2CCR	I^2C Data Register Reserved I^2C (7 Bits) Slave Address Register I^2C Clock Control Register I^2C Status Register 2 I^2C Status Register 1 I^2C Control Register	00h 00h 00h 00h 00h 00h	R/W R/W R/W Read only Read only R/W
0060h to 007Fh	Reserved Area (32 bytes)				

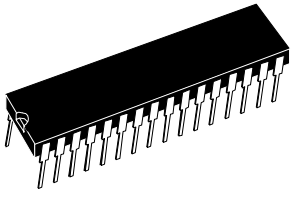
Notes

ST72251

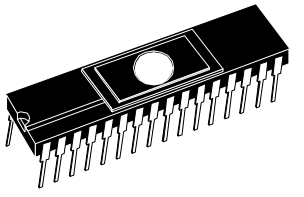
8-BIT MCU WITH 4 TO 8K ROM/OTP/EPROM, 256 BYTES RAM, ADC, WDG, SPI, I²C AND 2 TIMERS

PRELIMINARY DATA

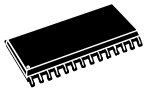
- User Program Memory (ROM/OTP/EPROM): 4 to 8K bytes
- Data RAM: 256 bytes, including 64 bytes of stack
- Master Reset and Power-On Reset
- Run, Wait, Slow, Halt and RAM Retention modes
- 22 multifunctional bidirectional I/O lines:
  - 22 programmable interrupt inputs
  - 8 high sink outputs
  - 6 Analog alternate inputs
  - 16 Alternate Functions
  - EMI filtering
- Programmable watchdog (WDG)
- Two 16-bit Timers, each featuring:
  - 2 Input Captures
  - 2 Output Compares
  - External Clock input (on Timer A only)
  - PWM and Pulse Generator modes
- Synchronous Serial Peripheral Interface (SPI)
- Full I²C multiple Master/Slave interface
- 8-bit Analog-to-Digital converter (6 channels)
- 8-bit Data Manipulation
- 63 Basic Instructions
- 17 main Addressing Modes
- 8 x 8 Unsigned Multiply Instruction
- True Bit Manipulation
- Complete Development Support on PC/DOS-WINDOWS™ Real-Time Emulator
- Full Software Package on DOS/WINDOWS™ (C-Compiler, Cross-Assembler, Debugger)



PSDIP32



CSDIP32W



PSO28

Device Summary

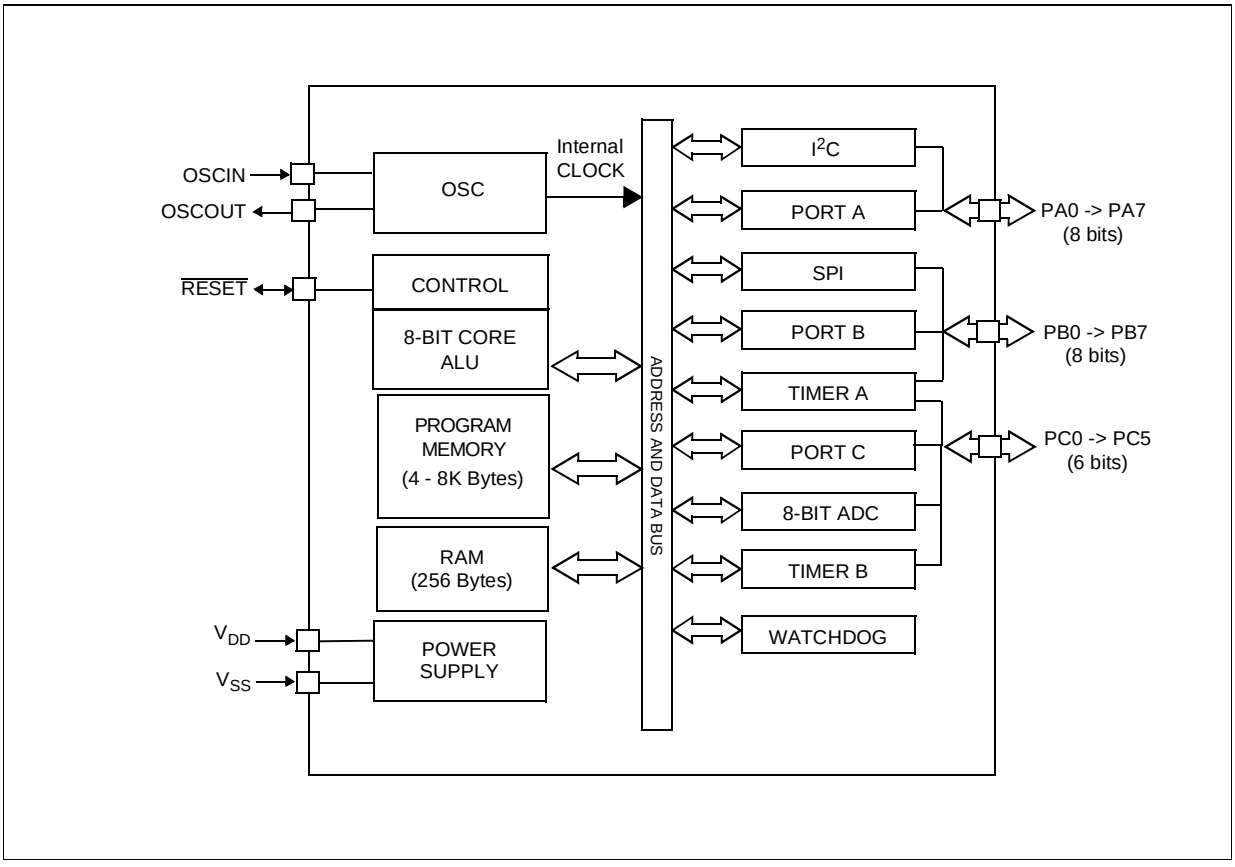
Features	ST72251G1	ST72251G2
Program Memory - bytes	4K	8K
RAM (stack) - bytes	256 (64)	
Peripherals	Watchdog, Timers, SPI, I²C, ADC	
Operating Supply	3 to 6 V	
CPU Frequency	8MHz max (16MHz oscillator)	
Temperature Range	- 40°C to + 85°C	
Package	SO28 - SDIP32	

1 GENERAL DESCRIPTION

1.1 INTRODUCTION

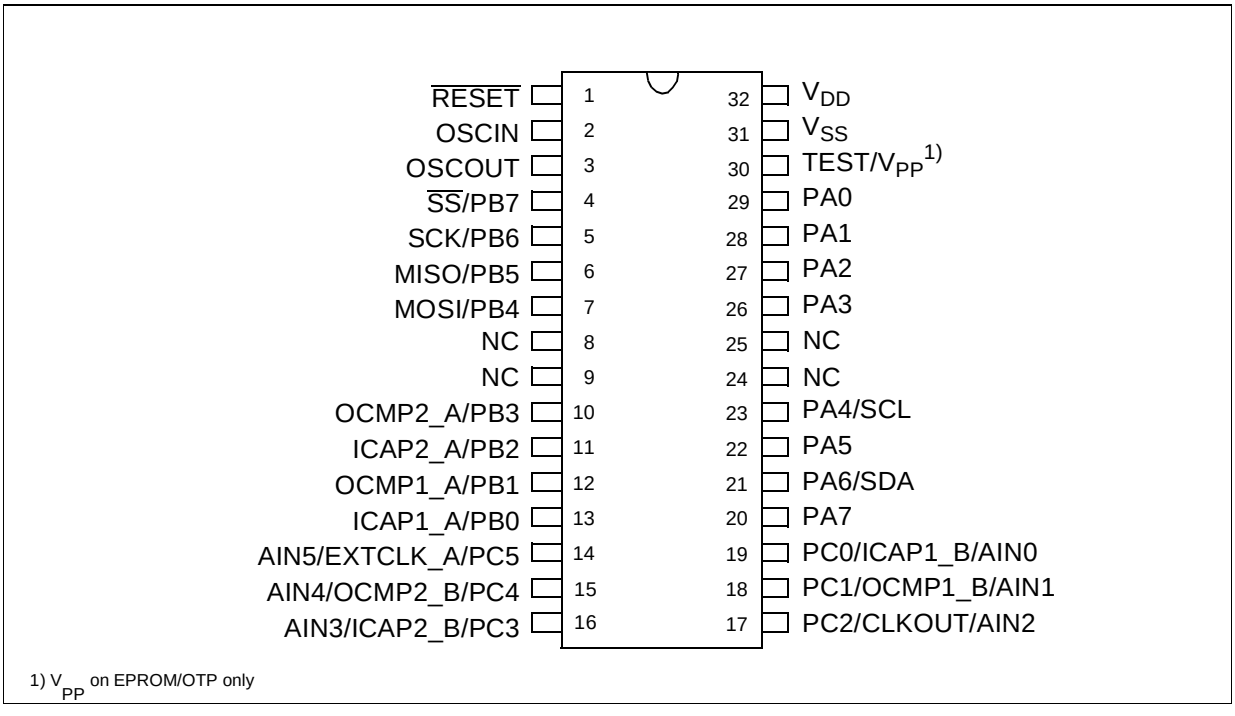
The ST72251 HCMOS Microcontroller Unit is a member of the ST7 family of Microcontrollers. The device is based on an industry-standard 8-bit core and features an enhanced instruction set. The device normally operates at a 16MHz oscillator frequency. Under software control, the ST72251 may be placed in either WAIT, SLOW or HALT modes, thus reducing power consumption. The enhanced instruction set and addressing modes afford real programming potential. In addition to standard 8-bit data management, the ST72251 features true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes on the whole memory. The device includes an on-chip oscillator, CPU, program memory (ROM/OTP/EPROM versions), RAM, 22 I/O lines and the following on-chip peripherals: Analog-to-Digital converter (ADC) with 6 multiplexed analog inputs, industry standard synchronous SPI serial interface, I^2C multiple Master/ Slave interface, digital Watchdog, two independent 16-bit Timers, one featuring an External Clock Input, and both featuring Pulse Generator capabilities, 2 Input Captures and 2 Output Compares.

Figure 1. ST72251 Block Diagram



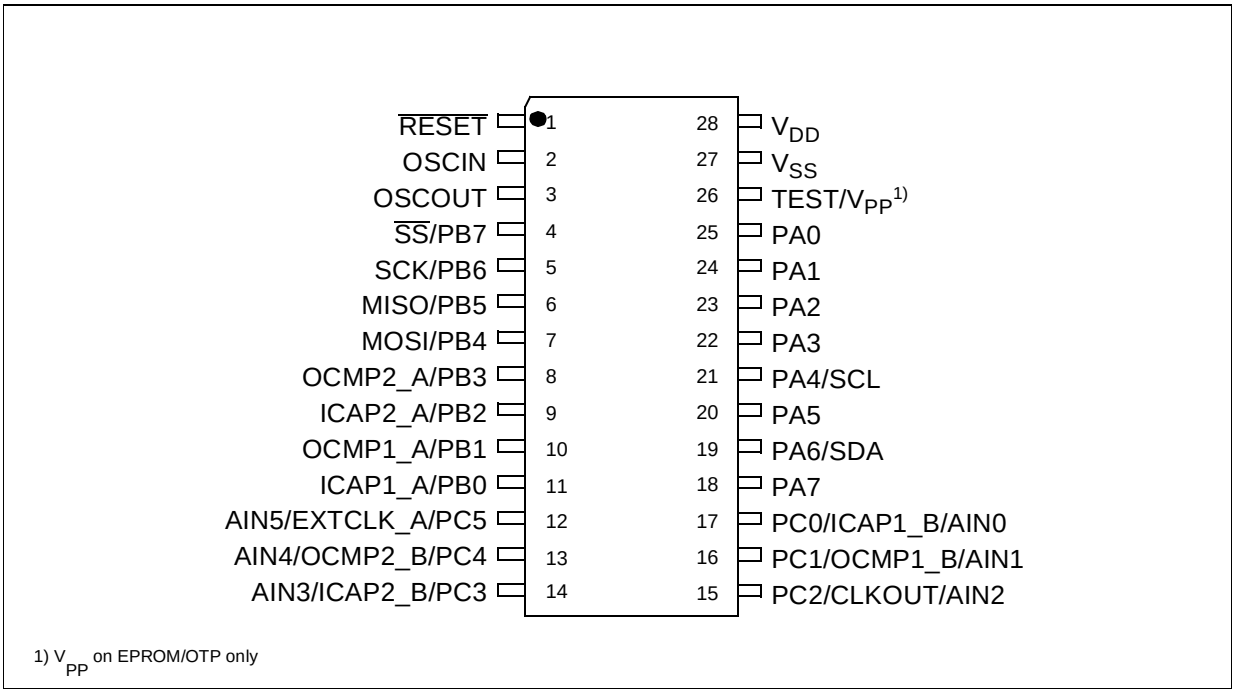
1.2 PIN DESCRIPTION

Figure 2. ST72251 Pinout (SDIP32)



1) V_{PP} on EPROM/OTP only

Figure 3. ST72251 Pinout (SO28)



1) V_{PP} on EPROM/OTP only

Table 1. ST72251 Pin Configuration

Pin n° SDIP32	Pin n° SO28	Pin Name	Type	Description	Remarks
1	1	$\overline{\text{RESET}}$	I/O	Bidirectional. Active low. Top priority non maskable interrupt.	
2	2	OSCIN	I	Input/Output Oscillator pin. These pins connect a parallel-resonant crystal, or an external source to the on-chip oscillator.	
3	3	OSCOUT	O		
4	4	PB7/$\overline{\text{SS}}$	I/O	Port B7 or SPI Slave Select (active low)	External Interrupt: EI1
5	5	PB6/SCK	I/O	Port B6 or SPI Serial Clock	External Interrupt: EI1
6	6	PB5/MISO	I/O	Port B5 or SPI Master In/ Slave Out Data	External Interrupt: EI1
7	7	PB4/MOSI	I/O	Port B4 or SPI Master Out / Slave In Data	External Interrupt: EI1
8		NC		Not Connected	
9		NC		Not Connected	
10	8	PB3/OCMP2_A	I/O	Port B3 or TimerA Output Compare 2	External Interrupt: EI1
11	9	PB2/ICAP2_A	I/O	Port B2 or TimerA Input Capture 2	External Interrupt: EI1
12	10	PB1/OCMP1_A	I/O	Port B1 or TimerA Output Compare 1	External Interrupt: EI1
13	11	PB0/ICAP1_A	I/O	Port B0 or TimerA Input Capture 1	External Interrupt: EI1
14	12	PC5/EXTCLK_A/AIN5	I/O	Port C5 or TimerA Input Clock or ADC Analog Input 5	External Interrupt: EI1
15	13	PC4/OCMP2_B/AIN4	I/O	Port C4 or TimerB Output Compare 2 or ADC Analog Input 4	External Interrupt: EI1
16	14	PC3/ICAP2_B/AIN3	I/O	Port C3 or TimerB Input Capture 2 or ADC Analog Input 3	External Interrupt: EI1
17	15	PC2/CLKOUT/AIN2	I/O	Port C2 or Internal Clock Frequency output or ADC Analog Input 2. Clockout is driven by the MCO bit of the miscellaneous register.	External Interrupt: EI1
18	16	PC1/OCMP1_B/AIN1	I/O	Port C1 or TimerB Output Compare 1 or ADC Analog Input 1	External Interrupt: EI1
19	17	PC0/ICAP1_B/AIN0	I/O	Port C0 or TimerB Input Capture 1 or ADC Analog Input 0	External Interrupt: EI1
20	18	PA7	I/O	Port A7, High Sink	External Interrupt: EI0
21	19	PA6/SDA	I/O	Port A6 or I^2C Data, High Sink	External Interrupt: EI0
22	20	PA5	I/O	Port A5, High Sink	External Interrupt: EI0
23	21	PA4/SCL	I/O	Port A4 or I^2C Clock, High Sink	External Interrupt: EI0
24		NC		Not Connected	
25		NC		Not Connected	
26	22	PA3	I/O	Port A3, High Sink	External Interrupt: EI0
27	23	PA2	I/O	Port A2, High Sink	External Interrupt: EI0
28	24	PA1	I/O	Port A1, High Sink	External Interrupt: EI0
29	25	PA0	I/O	Port A0, High Sink	External Interrupt: EI0
30	26	TEST/V_{PP}	S	Test mode pin (should be tied low in user mode). In the EPROM programming mode, this pin acts as the programming voltage input V_{PP}.	
31	27	V_{SS}	S	Ground	
32	28	V_{DD}	S	Main power supply	

1.3 MEMORY MAP

Figure 4. Memory Map

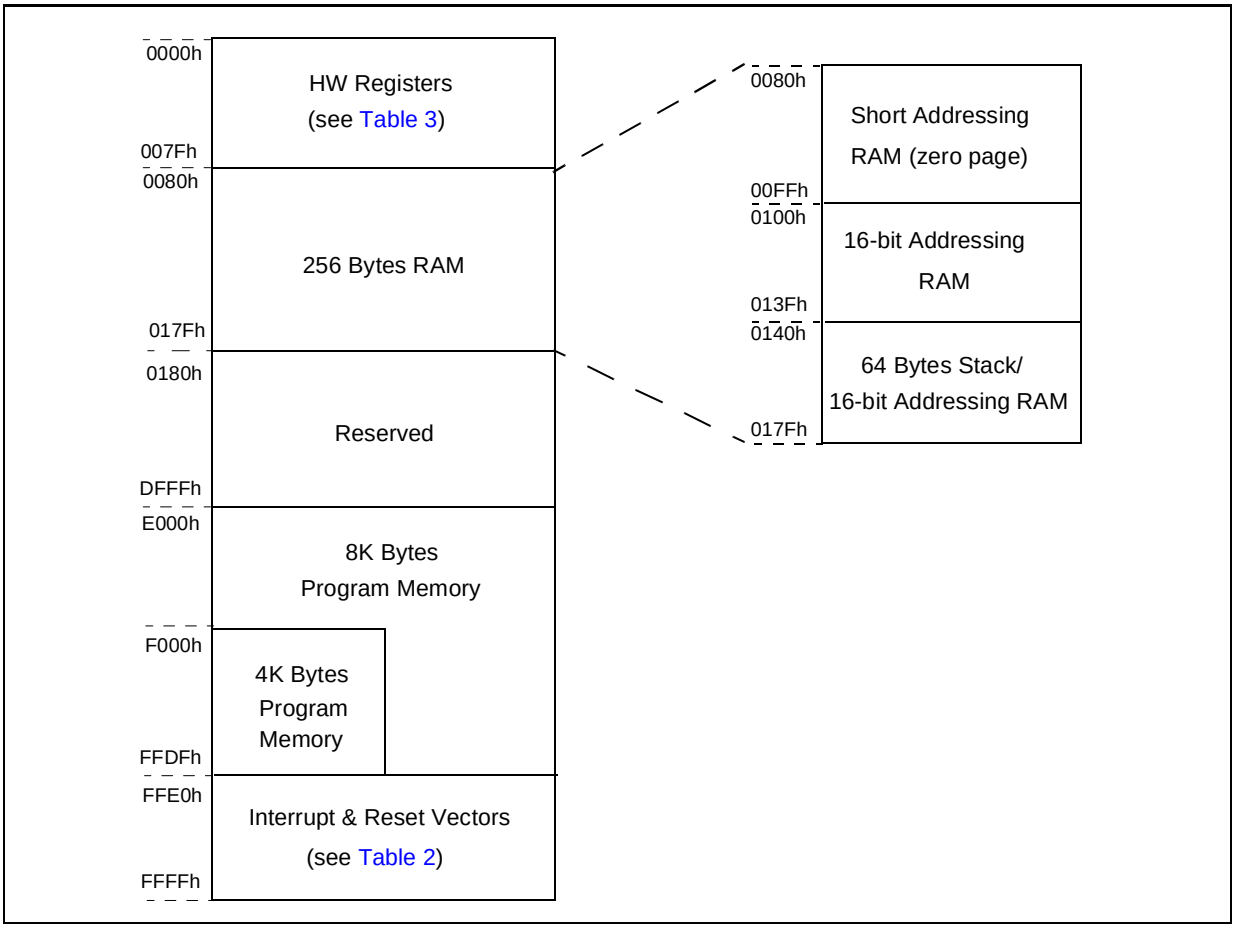


Table 2. Interrupt Vector Map

Vector Address	Description	Remarks
FFE0-FFE1h	Not Used	
FFE2-FFE3h	Not Used	
FFE4-FFE5h	I^2C Interrupt Vector	Internal Interrupt
FFE6-FFE7h	Not Used	
FFE8-FFE9h	Not Used	
FFEA-FFEBh	Not Used	
FFEC-FFEDh	Not Used	
FFEE-FFEFh	TIMER B Interrupt Vector	Internal Interrupt
FFF0-FFF1h	Not Used	
FFF2-FFF3h	TIMER A Interrupt Vector	Internal Interrupt
FFF4-FFF5h	SPI Interrupt Vector	Internal Interrupt
FFF6-FFF7h	Not Used	
FFF8-FFF9h	External Interrupt Vector EI1	External Interrupt
FFFA-FFFBh	External Interrupt Vector EI0	External Interrupt
FFFC-FFFDh	TRAP (software) Interrupt Vector	CPU Interrupt
FFFE-FFFFh	RESET Vector	

Table 3. Hardware Register Memory Map

Address	Block Name	Register Label	Register name	Reset Status	Remarks
0000h	Port C	PCDR	Data Register	00h	R/W (1)
0001h		PCDDR	Data Direction Register	00h	R/W (1)
0002h		PCOR	Option Register	00h	R/W (1)
0003h	Reserved Area (1 Byte)				
0004h	Port B	PBDR	Data Register	00h	R/W
0005h		PBDDR	Data Direction Register	00h	R/W
0006h		PBOR	Option Register	00h	R/W
0007h	Reserved Area (1 Byte)				
0008h	Port A	PADR	Data Register	00h	R/W
0009h		PADDR	Data Direction Register	00h	R/W
000Ah		PAOR	Option Register	00h	R/W
000Bh to 001Fh	Reserved Area (21 Bytes)				
0020h		MISCR	Miscellaneous Register	00h	
0021h	SPI	SPIDR	Data I/O Register	xxh	R/W
0022h		SPICR	Control Register	0xh	R/W
0023h		SPISR	Status Register	00h	Read Only
0024h	WDG	WDGCR	Watchdog Control register	7Fh	R/W
0025h to 0027h	Reserved Area (3 Bytes)				
0028h	I^2C	I2CCR	Control Register	00h	R/W
0029h		I2CSR1	Status Register 1	00h	Read Only
002Ah		I2CSR2	Status Register 2	00h	Read Only
002Bh		I2CCCR	Clock Control Register	00h	R/W
002Ch		I2COAR1	Own Address Register 1	00h	R/W
002Dh		I2COAR2	Own Address Register 2	00h	R/W
002Eh		I2CDR	Data Register	00h	R/W
002Fh 0030h	Reserved Area (2 Bytes)				
0031h	Timer A	TACR2	Control Register2	00h	R/W
0032h		TACR1	Control Register1	00h	R/W
0033h		TASR	Status Register	00h	Read Only
0034h-0035h		TAIC1HR	Input Capture1 High Register	xxh	Read Only
		TAIC1LR	Input Capture1 Low Register	xxh	Read Only
0036h-0037h		TAOC1HR	Output Compare1 High Register	80h	R/W
		TAOC1LR	Output Compare1 Low Register	00h	R/W
0038h-0039h		TACHR	Counter High Register	FFh	Read Only
		TACLR	Counter Low Register	FCh	Read Only
003Ah-003Bh		TAACHR	Alternate Counter High Register	FFh	Read Only
		TAACLR	Alternate Counter Low Register	FCh	Read Only
003Ch-003Dh		TAIC2HR	Input Capture2 High Register	xxh	Read Only
		TAIC2LR	Input Capture2 Low Register	xxh	Read Only
003Eh-003Fh		TAOC2HR	Output Compare2 High Register	80h	R/W
		TAOC2LR	Output Compare2 Low Register	00h	R/W
0040h	Reserved Area (1 Byte)				

Address	Block Name	Register Label	Register name	Reset Status	Remarks
0041h		TBCR2	Control Register2	00h	R/W
0042h		TBCR1	Control Register1	00h	R/W
0043h		TBSR	Status Register	00h	Read Only
0044h-0045h		TBIC1HR	Input Capture1 High Register	xxh	Read Only
		TBIC1LR	Input Capture1 Low Register	xxh	Read Only
0046h-0047h		TBOC1HR	Output Compare1 High Register	80h	R/W
		TBOC1LR	Output Compare1 Low Register	00h	R/W
0048h-0049h	Timer B	TBCHR	Counter High Register	FFh	Read Only
		TBCLR	Counter Low Register	FCh	Read Only
004Ah-004Bh		TBACHR	Alternate Counter High Register	FFh	Read Only
		TBACLR	Alternate Counter Low Register	FCh	Read Only
004Ch-004Dh		TBIC2HR	Input Capture2 High Register	xxh	Read Only
		TBIC2LR	Input Capture2 Low Register	xxh	Read Only
004Eh-004Fh		TBOC2HR	Output Compare2 High Register	80h	R/W
		TBOC2LR	Output Compare2 Low Register	00h	R/W
0050h to 006Fh	Reserved Area (32 Bytes)				
0070h	ADC	ADCDR	Data Register	00h	Read Only
0071h		ADCCSR	Control/Status Register	00h	R/W
0072h to 007Fh	Reserved Area (14 Bytes)				

Note 1: The bits corresponding to unavailable pins are forced to zero by hardware.

Notes:

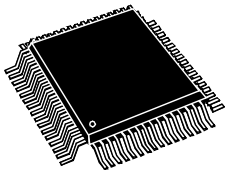
ST72511

8-BIT MCU WITH 16K TO 32K ROM/OTP/EPROM, 512 BYTES TO 1K RAM, CAN, ADC, PWM, SPI, SCI AND 2 TIMERS

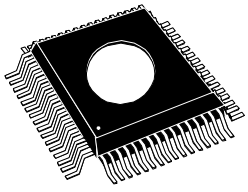
PRODUCT PREVIEW

- User ROM/OTP/EPROM: 16K to 32K bytes
- Data RAM: 512 to 1K bytes, including 256 bytes stack
- Master Reset and Power-On Reset
- Run, Wait, and Slow modes
- CAN 2.0B passive interface
- 44 multifunctional bidirectional I/O lines:
  - 15 Programmable Interrupt inputs
  - 8 Analog alternate inputs
  - 4 high sink outputs
  - 17 Alternate functions
  - EMI filtering
- Hardware Watchdog (WDG)
- Two 16-bit Timers, each featuring:
  - 2 Input Captures(1)
  - 2 Output Compares(1)
  - External Clock input (on Timer A)
  - PWM and Pulse Generator modes
- 8-bit Analog-to-Digital Converter
- Two 10-bit Digital to Analog Converter channels with PWM output
- Synchronous Serial Peripheral Interface (SPI)
- Asynchronous Serial Communications Interface (SCI)
- 8-bit Data Manipulation
- 63 basic Instructions and 17 main Addressing Modes
- 8 x 8 Unsigned Multiply Instruction
- True Bit Manipulation
- Complete Development Support on DOS/ WINDOWS™ Real-Time Emulator
- Full Software Package on DOS/WINDOWS™ (C-Compiler, Cross-Assembler, Debugger)

Note 1. One only on Timer A.



TQFP64



CQFP64W

Device Summary

Features	ST72511R4	ST72511R6
ROM - bytes	16K	32K
RAM (stack) - bytes	512 (256)	1024 (256)
Peripherals	CAN, ADC, Watchdog, 2 Timers, PWM, SPI, SCI	
Operating Supply	4.5 to 5.5 V	
Oscillator Frequency	16MHz max	
Temperature Range	- 40°C to + 85°C	
Package	TQFP64	
OTP/EPROM Devices	ST72T511R6 / ST72E511R6	

1 GENERAL DESCRIPTION

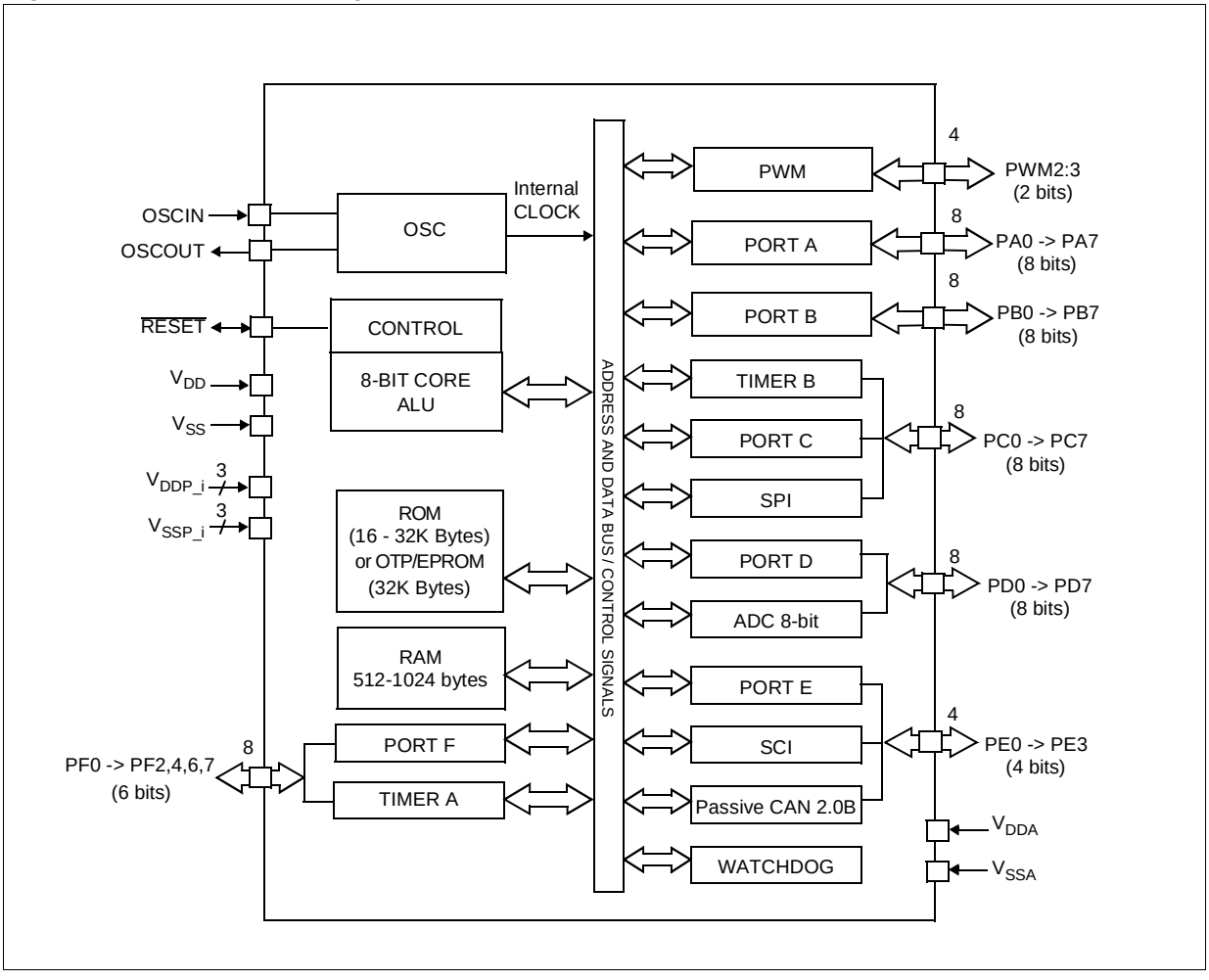
1.1 INTRODUCTION

The ST72511 HCMOS Microcontroller Unit (MCU) is a member of the ST7 family with an on-chip Controller Area Network (CAN) interface. The CAN controller is compatible with the CAN 2.0B specification (passive).

The device is based on an industry-standard 8-bit core and features an enhanced instruction set. The device is normally operated at a 16MHz oscillator frequency. Under software control, the ST72511 may be placed in either Wait or Slow modes, thus reducing power consumption. The enhanced instruction set and addressing modes provide real programming potential. In addition to standard 8-bit data management, the ST72511 features true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes on the whole memory. The device includes a low consumption and fast start on-chip oscillator, CPU, ROM/OTP/EPROM, RAM, 44 I/O lines and the following on-chip peripherals: CAN Controller, Analog-to-Digital converter (ADC) with 8 multiplexed analog inputs, industry standard synchronous SPI and asynchronous SCI serial interfaces, digital Watchdog, two independent 16-bit Timers, one featuring an External Clock Input. Timer B features Pulse Generator capabilities, 2 Input Captures and 2 Output Compares. Timer A has the same features as Timer B but with 1 Input Capture and 1 Output Compare pin.

The ST72E511 is the EPROM version of the ST72511 in a CQFP64 package.

Figure 1. ST72511 Block Diagram



1.2 PIN DESCRIPTION

Figure 2. 64-Pin Thin QFP Package Pinout

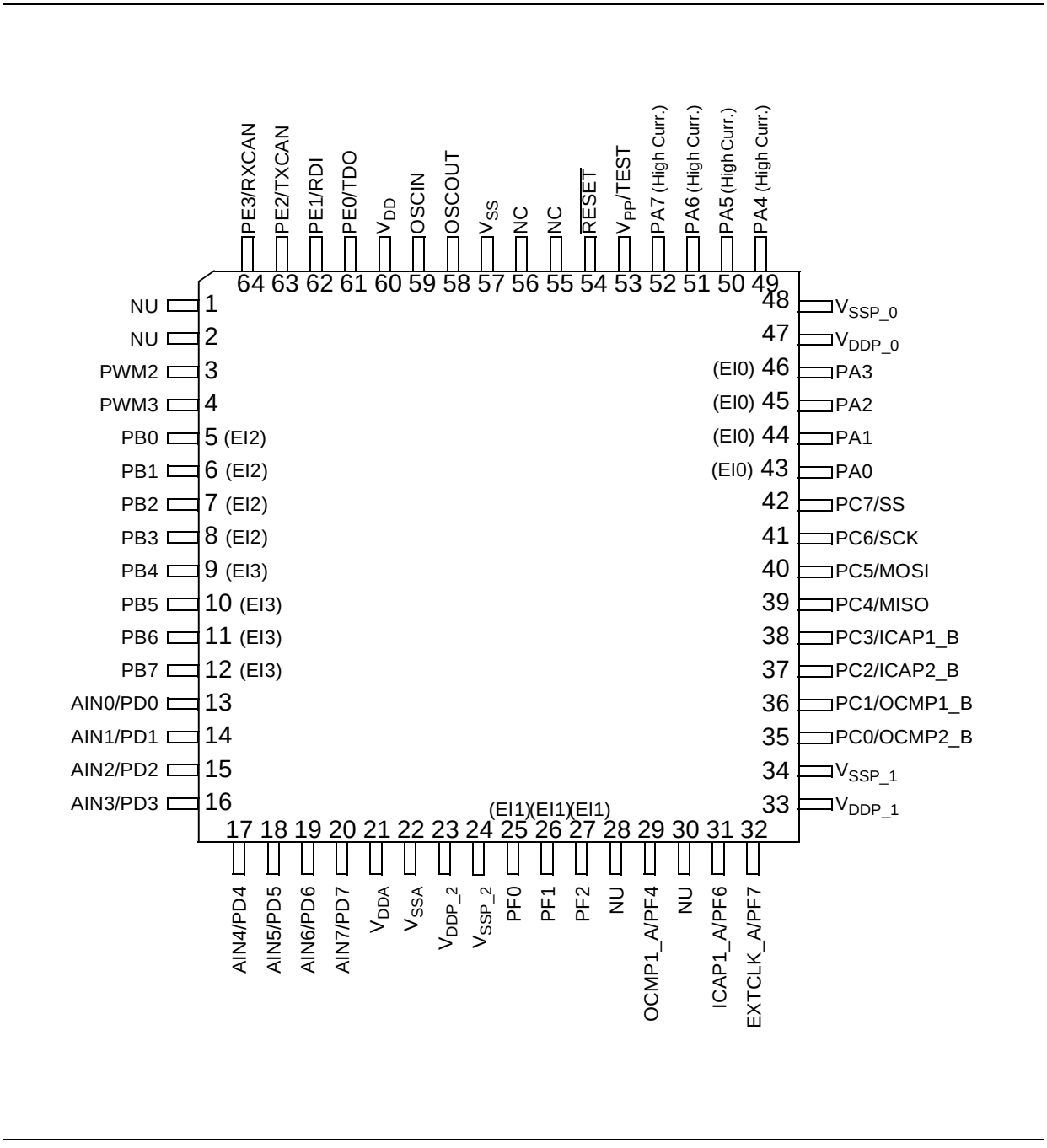


Table 1. Pin Description

Pin	Pin Name	Type	Description	Remarks
1	NU		Non user pin. Must be left unconnected.	
2	NU		Non user pin. Must be left unconnected.	
3	PWM2	O	PWM Output 2	
4	PWM3	O	PWM Output 3	
5	PB0	I/O	Port B0	External Interrupt: EI2
6	PB1	I/O	Port B1	External Interrupt: EI2
7	PB2	I/O	Port B2	External Interrupt: EI2
8	PB3	I/O	Port B3	External Interrupt: EI2
9	PB4	I/O	Port B4	External Interrupt: EI3
10	PB5	I/O	Port B5	External Interrupt: EI3
11	PB6	I/O	Port B6	External Interrupt: EI3
12	PB7	I/O	Port B7	External Interrupt: EI3
13	PD0/AIN0	I/O	Port D0 or ADC Analog Input 0	
14	PD1/AIN1	I/O	Port D1 or ADC Analog Input 1	
15	PD2/AIN2	I/O	Port D2 or ADC Analog Input 2	
16	PD3/AIN3	I/O	Port D3 or ADC Analog Input 3	
17	PD4/AIN4	I/O	Port D4 or ADC Analog Input 4	
18	PD5/AIN5	I/O	Port D5 or ADC Analog Input 5	
19	PD6/AIN6	I/O	Port D6 or ADC Analog Input 6	
20	PD7/AIN7	I/O	Port D7 or ADC Analog Input 7	
21	V_{DDA}	S	Power Supply for analog peripheral (ADC)	
22	V_{SSA}	S	Ground for analog peripheral (ADC)	
23	V_{DDP_2}	S	Power Supply for Output Buffers (Ports B&E and PWM outputs)	
24	V_{SSP_2}	S	Ground for Output Buffers (Ports B&E and PWM outputs)	
25	PF0	I/O	Port F0	External Interrupt: EI1
26	PF1	I/O	Port F1	External Interrupt: EI1
27	PF2	I/O	Port F2	External Interrupt: EI1
28	NU		Non user pin. Must be left unconnected.	
29	PF4/OCMP1_A	I/O	Port F4 or Timer A Output Compare 1	
30	NU		Non user pin. Must be left unconnected.	
31	PF6/ICAP1_A	I/O	Port F6 or Timer A Input Capture 1	
32	PF7/EXTCLK_A	I/O	Port F7 or External Clock on Timer A	
33	V_{DDP_1}	S	Power Supply for Output Buffers (Ports C & F)	
34	V_{SSP_1}	S	Ground for Output Buffers (Ports C & F)	
35	PC0/OCMP2_B	I/O	Port C0 or Timer B Output Compare 2	
36	PC1/OCMP1_B	I/O	Port C1 or Timer B Output Compare 1	
37	PC2/ICAP2_B	I/O	Port C2 or Timer B Input Capture 2	
38	PC3/ICAP1_B	I/O	Port C3 or Timer B Input Capture 1	

Pin	Pin Name	Type	Description	Remarks
39	PC4/MISO	I/O	Port C4 or SPI Master In / Slave Out Data	
40	PC5/MOSI	I/O	Port C5 or SPI Master Out / Slave In Data	
41	PC6/SCK	I/O	Port C6 or SPI Serial Clock	
42	PC7/$\overline{SS}$	I/O	Port C7 or SPI Slave Select (active low)	
43	PA0	I/O	Port A0	External Interrupt: EI0
44	PA1	I/O	Port A1	External Interrupt: EI0
45	PA2	I/O	Port A2	External Interrupt: EI0
46	PA3	I/O	Port A3	External Interrupt: EI0
47	V_{DDP_0}	S	Power Supply for Output buffers (PA0 to PA3)	
48	V_{SSP_0}	S	Ground for Output buffers (Port A)	
49	PA4	I/O	Port A4	High Current
50	PA5	I/O	Port A5	High Current
51	PA6	I/O	Port A6	High Current
52	PA7	I/O	Port A7	High Current
53	TEST/V_{PP}(1)	S	Test mode pin. In EPROM programming mode, this pin acts as the programming voltage input V_{PP}.	This pin should be tied low in user mode
54	$\overline{RESET}$	I/O	Bidirectional. Active low. Top priority non maskable interrupt.	
55	NC		Not Connected	
56	NC		Not Connected	
57	V_{SS}	S	Ground	
58	OSCOUT	I/O	Input/Output Oscillator pin. These pins connect a parallel resonant crystal, or an external source to the on-chip oscillator.	
59	OSCIN	I/O		
60	V_{DD}	S	Main power supply	
61	PE0/TDO	I/O	Port E0 or SCI Transmit Data Out	
62	PE1/RDI	I/O	Port E1 or SCI Receive Data In	
63	PE2/TXCAN	I	Port E2 or CAN Transmit Data Output	
64	PE3/RXCAN	I/O	Port E3 or CAN Receive Data Input	

Note 1: V_{PP} on EPROM/OTP only.

1.3 MEMORY MAP

Figure 3. Program Memory Map

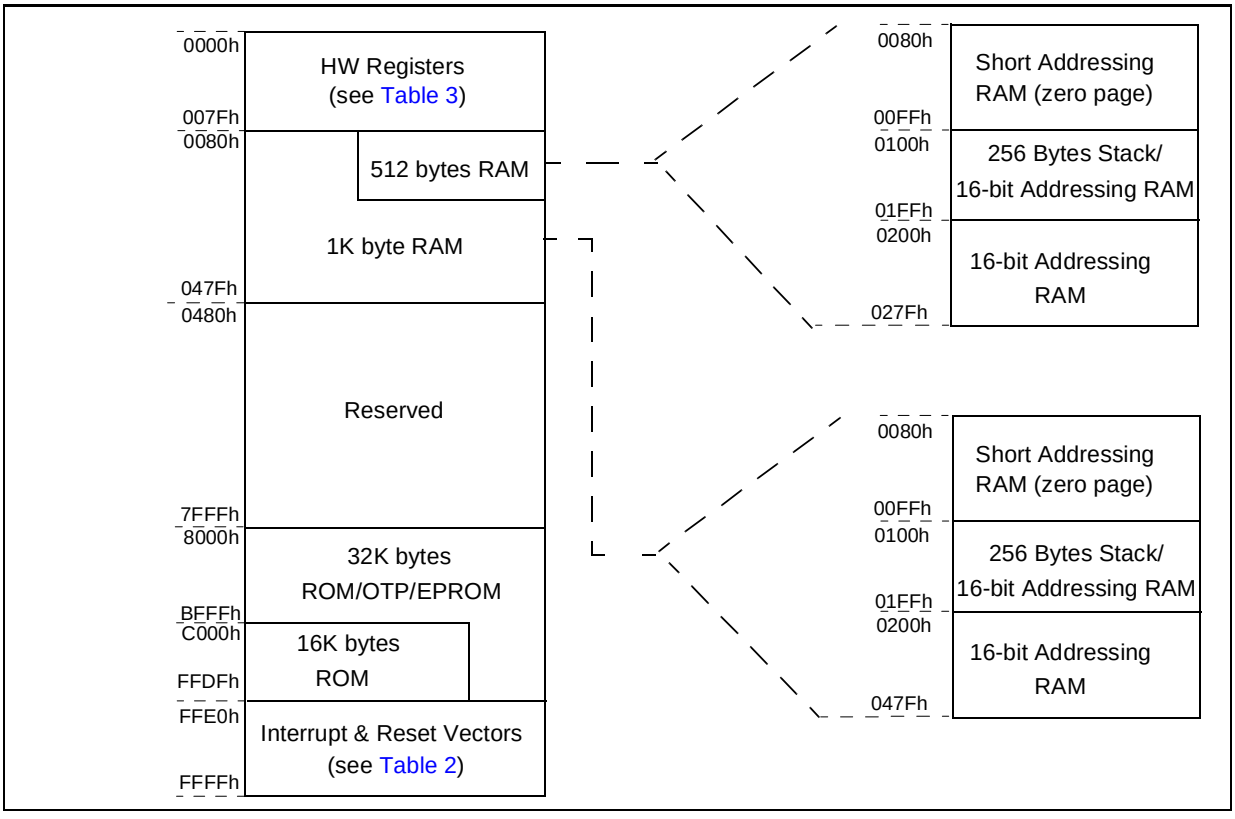


Table 2. Interrupt Vector Map

Vector Address	Description	Remarks
FFE0-FFE1h	Not Used	
FFE2-FFE3h	Not Used	
FFE4-FFE5h	EEPROM Programming Interrupt	Internal Interrupt
FFE6-FFE7h	SCI Interrupt Vector	Internal Interrupt
FFE8-FFE9h	TIMER B Interrupt Vector	Internal Interrupt
FFEA-FFEBh	TIMER A Interrupt Vector	Internal Interrupt
FFEC-FFEDh	SPI Interrupt Vector	Internal Interrupt
FFEE-FFEFh	CAN Interrupt Vector	Internal Interrupt
FFF0-FFF1h	External Interrupt Vector EI3 (PB4:PB7)	External Interrupt
FFF2-FFF3h	External Interrupt Vector EI2 (PB0:PB3)	External Interrupt
FFF4-FFF5h	External Interrupt Vector EI1 (PF0:PF2)	External Interrupt
FFF6-FFF7h	External Interrupt Vector EI0 (PA0:PA3)	External Interrupt
FFF8-FFF9h	Not Used	
FFFA-FFFBh	Not Used	
FFFC-FFFDh	TRAP (software) Interrupt Vector	CPU Interrupt
FFFE-FFFFh	RESET Vector	

Table 3. Hardware Register Memory Map

Address	Block	Register Label	Register name	Reset Status	Remarks
0000h 0001h 0002h 0003h	Port A	PADR PADDR PAOR	Data Register Data Direction Register Option Register Not Used	00h 00h 00h	R/W R/W R/W Absent
0004h 0005h 0006h 0007h	Port C	PCDR PCDDR	Data Register Data Direction Register Not Used Not Used	00h 00h	R/W R/W Absent Absent
0008h 0009h 000Ah 000Bh	Port B	PBDR PBDDR PBOR	Data Register Data Direction Register Option Register Not Used	00h 00h 00h	R/W R/W R/W Absent
000Ch 000Dh 000Eh 000Fh	Port E	PEDR PEDDR	Data Register Data Direction Register Not Used Not Used	00h 00h	R/W(1) R/W(1) Absent Absent
0010h 0011h 0012h 0013h	Port D	PDDR PDDDR	Data Register Data Direction Register Not Used Not Used	00h 00h	R/W R/W Absent Absent
0014h 0015h 0016h 0017h	Port F	PFDR PFDDR PFOR	Data Register Data Direction Register Option Register Not Used	00h 00h 00h	R/W R/W R/W Absent
0018h to 001Fh	Reserved Area (8 Bytes)				
0020h		MISCR	Miscellaneous Register	00h	
0021h 0022h 0023h	SPI	SPIDR SPICR SPISR	SPI Data I/O Register SPI Control Register SPI Status Register	xxh 0xh 00h	R/W R/W Read Only
0024h 0025h 0026h 0027h 0028h 0029h	PWMB	PWM0 BRM10 PWM1 PWM2 BRM32 PWM3	Pulse Binary Weight Register 0 BRM Register 10 Pulse Binary Weight Register 1 Pulse Binary Weight Register 2 BRM Register 32 Pulse Binary Weight Register 3	80h 00h 80h 80h 00h 80h	R/W R/W R/W R/W R/W R/W
002Ah 002Bh	WDG	WDGCR	Watchdog Control Register Not used	7Fh	R/W
002Ch to 0030h	Reserved Area (5 Bytes)				
0031h 0032h 0033h 0034h-0035h 0036h-0037h	Timer A	TACR2 TACR1 TASR TAIC1HR TAIC1LR TAOC1HR TAOC1LR	Control Register2 Control Register1 Status Register Input Capture1 High Register Input Capture1 Low Register Output Compare1 High Register Output Compare1 Low Register	00h 00h xxh xxh xxh 80h 00h	R/W R/W Read Only Read Only Read Only R/W R/W

Address	Block	Register Label	Register name	Reset Status	Remarks
0038h-0039h	Timer A	TACHR	Counter High Register	FFh	Read Only
		TACLR	Counter Low Register	FCh	Read Only
003Ah-003Bh		TAACHR	Alternate Counter High Register	FFh	Read Only
		TAACLR	Alternate Counter Low Register	FCh	Read Only
003Ch-003Dh		TAIC2HR	Input Capture2 High Register	xxh	Read Only(2)
		TAIC2LR	Input Capture2 Low Register	xxh	Read Only(2)
003Eh-003Fh		TAOC2HR	Output Compare2 High Register	80h	R/W(2)
		TAOC2LR	Output Compare2 Low Register	00h	R/W(2)
0040h	Reserved Area				
0041h	Timer B	TBCR2	Control Register2	00h	R/W
0042h		TBCR1	Control Register1	00h	R/W
0043h		TBSR	Status Register	xxh	Read Only
0044h-0045h		TBIC1HR	Input Capture1 High Register	xxh	Read Only
		TBIC1LR	Input Capture1 Low Register	xxh	Read Only
0046h-0047h		TBOC1HR	Output Compare1 High Register	80h	R/W
		TBOC1LR	Output Compare1 Low Register	00h	R/W
0048h-0049h		TBCHR	Counter High Register	FFh	Read Only
		TBCLR	Counter Low Register	FCh	Read Only
004Ah-004Bh		TBACHR	Alternate Counter High Register	FFh	Read Only
		TBACLR	Alternate Counter Low Register	FCh	Read Only
004Ch-004Dh		TBIC2HR	Input Capture2 High Register	xxh	Read Only
		TBIC2LR	Input Capture2 Low Register	xxh	Read Only
004Eh-004Fh		TBOC2HR	Output Compare2 High Register	80h	R/W
		TBOC2LR	Output Compare2 Low Register	00h	R/W
0050h	SCI	SCISR	SCI Status Register	C0h	Read Only
0051h		SCIDR	SCI Data Register	xxh	R/W
0052h		SCIBRR	SCI Baud Rate Register	00x----xb	R/W
0053h		SCICR1	SCI Control Register 1	xxh	R/W
0054h		SCICR2	SCI Control Register 2	00h	R/W
0055h		SCIERPR	SCI Extended Receive Prescaler Register	00h	R/W
0056h			Reserved	---	Reserved
0057h		SCIETPR	SCI Extended Transmit Prescaler Register	00h	R/W
0058h to 0059h	Reserved Area (2 Bytes)				
005Ah	CAN	CANISR	CAN Interrupt Status Register	00h	R/W
005Bh		CANICR	CAN Interrupt Control Register	00h	R/W
005Ch		CANCSR	CAN Control/Status Register	00h	R/W
005Dh		CANBRPR	CAN Baud Rate Prescaler Register	00h	R/W
005Eh		CANBTR	CAN Bit Timing Register	23h	R/W
005Fh		CANPSR	CAN Page Selection	00h	R/W
0060h to 006Fh			CAN First address to last address of PAGE X	--	
0070h to 007Fh	Reserved Area (16 Bytes)				

Notes:

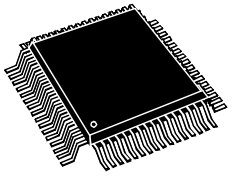
1. The bits corresponding to unavailable pins are forced to zero by hardware.
2. External pin not available.

ST72531

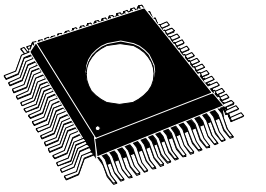
8-BIT MCU WITH 16K TO 32K ROM/OTP/EPROM, 256 BYTES EEPROM, 512 TO 1K RAM, CAN, ADC, PWM, SPI, SCI, 2 TIMERS

PRODUCT PREVIEW

- User ROM/OTP/EPROM: 16K to 32K bytes
- User EEPROM: 256 bytes
- Data RAM: 512 to 1K bytes, including 256 bytes stack
- Master Reset and Power-On Reset
- Run, Wait, and Slow modes
- CAN 2.0B passive interface
- 44 multifunctional bidirectional I/O lines:
  - 15 Programmable Interrupt inputs
  - 8 Analog alternate inputs
  - 4 high sink outputs
  - 17 Alternate functions
  - EMI filtering
- Hardware Watchdog (WDG)
- Two 16-bit Timers, each featuring:
  - 2 Input Captures(1)
  - 2 Output Compares(1)
  - External Clock input (on Timer A)
  - PWM and Pulse Generator modes
- 8-bit Analog-to-Digital Converter
- Two 10-bit Digital to Analog Converter channels with PWM output
- Synchronous Serial Peripheral Interface (SPI)
- Asynchronous Serial Communications Interface (SCI)
- 8-bit Data Manipulation
- 63 basic Instructions and 17 main Addressing Modes
- 8 x 8 Unsigned Multiply Instruction
- True Bit Manipulation
- Complete Development Support on DOS/ WINDOWS™ Real-Time Emulator
- Full Software Package on DOS/WINDOWS™ (C-Compiler, Cross-Assembler, Debugger)



TQFP64



CQFP64W

Device Summary

Features	ST72531R4	ST72531R6
ROM - bytes	16K	32K
EEPROM - bytes	256	
RAM (stack) - bytes	512 (256)	1024 (256)
Peripherals	CAN, ADC, Watchdog, 2 Timers, PWM, SPI, SCI	
Operating Supply	4.5 to 5.5 V	
Oscillator Frequency	16MHz max	
Temperature Range	- 40°C to + 85°C	
Package	TQFP64	
OTP/EPROM Devices	ST72T531R6 / ST72E531R6	

Note 1. One only on Timer A.

1 GENERAL DESCRIPTION

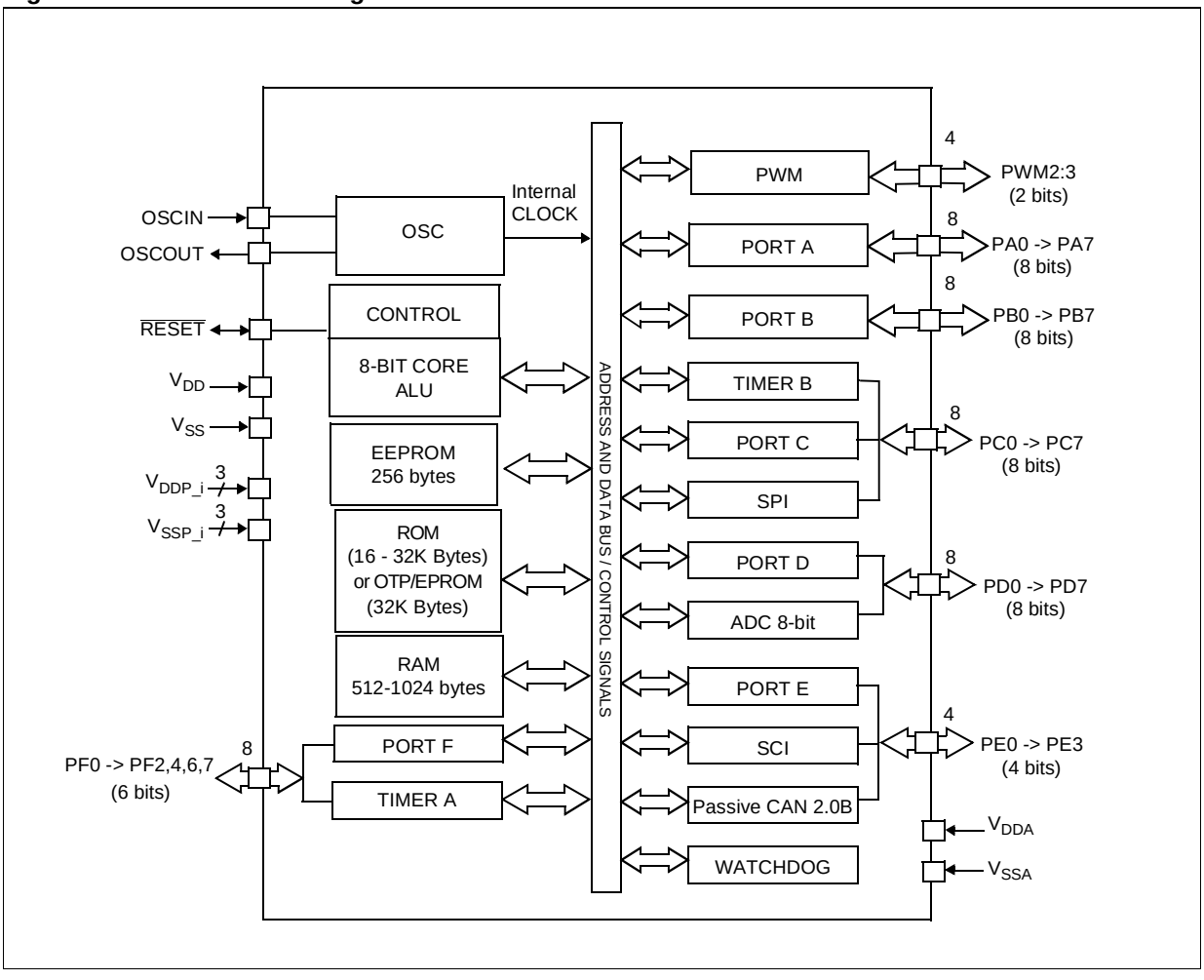
1.1 INTRODUCTION

The ST72531 HCMOS Microcontroller Unit (MCU) is a member of the ST7 family with an on-chip Controller Area Network (CAN) interface. The CAN controller is compatible with the CAN 2.0B specification (passive).

The device is based on an industry-standard 8-bit core and features an enhanced instruction set. The device is normally operated at a 16MHz oscillator frequency. Under software control, the ST72531 may be placed in either Wait or Slow modes, thus reducing power consumption. The enhanced instruction set and addressing modes provide real programming potential. In addition to standard 8-bit data management, the ST72531 features true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes. The device includes a low consumption and fast start on-chip oscillator, CPU, ROM/OTP/EPROM, EEPROM, RAM, 44 I/O lines and the following on-chip peripherals: CAN Controller, Analog-to-Digital converter (ADC) with 8 multiplexed analog inputs, industry standard synchronous SPI and asynchronous SCI serial interfaces, digital Watchdog, two independent 16-bit Timers. Timer B features Pulse Generator capabilities, 2 Input Captures and 2 Output Compares. Timer A has the same features as Timer B but with 1 Input Capture and 1 Output Compare pin.

The ST72E53x is the EPROM version of the ST72531 in a CQFP64 package.

Figure 1. ST72531 Block Diagram



1.2 PIN DESCRIPTION

Figure 2. 64-Pin Thin QFP Package Pinout

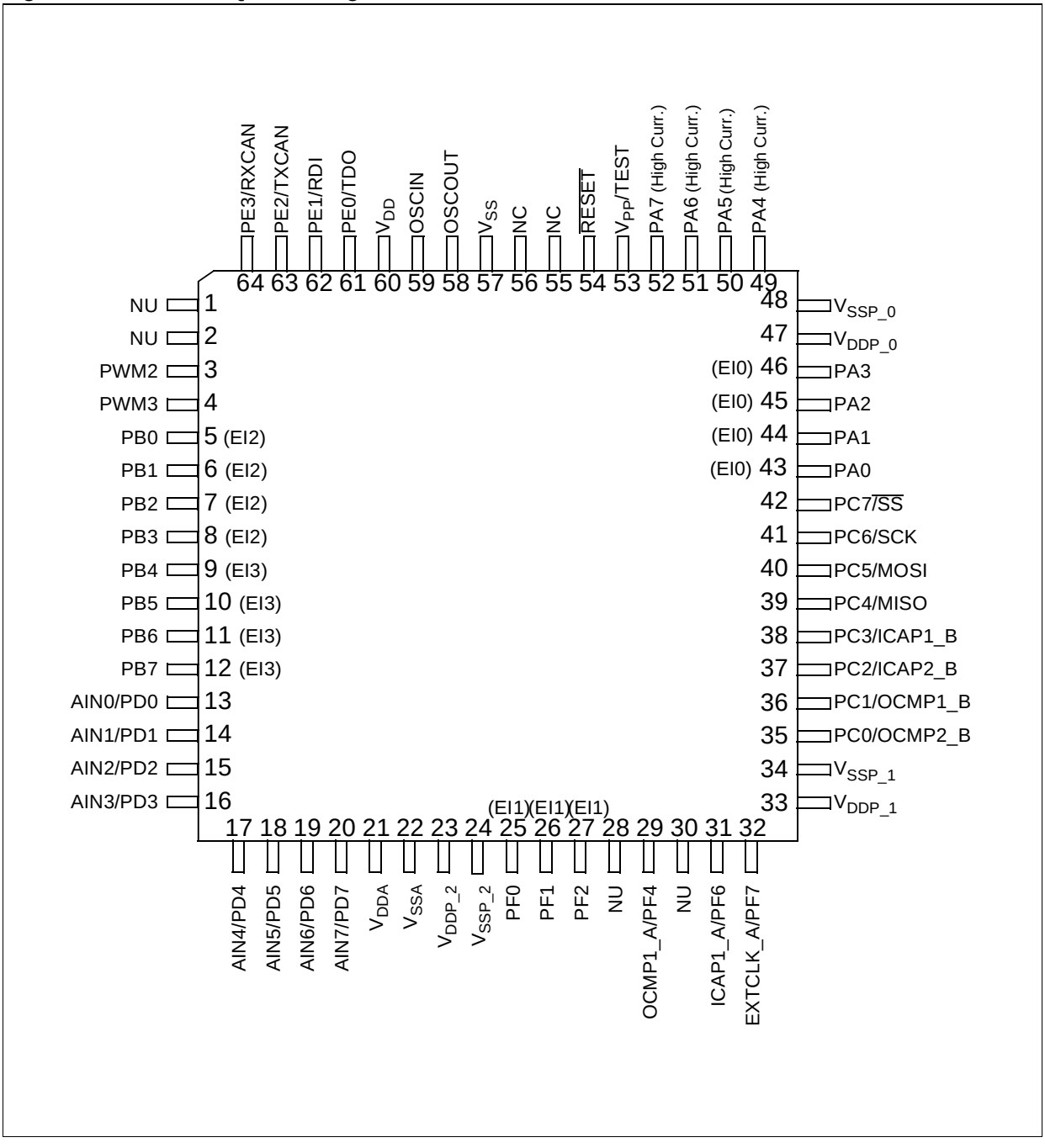


Table 1. Pin Description

Pin	Pin Name	Type	Description	Remarks
1	NU		Non user pin. Must be left unconnected.	
2	NU		Non user pin. Must be left unconnected.	
3	PWM2	O	PWM Output 2	
4	PWM3	O	PWM Output 3	
5	PB0	I/O	Port B0	External Interrupt: EI2
6	PB1	I/O	Port B1	External Interrupt: EI2
7	PB2	I/O	Port B2	External Interrupt: EI2
8	PB3	I/O	Port B3	External Interrupt: EI2
9	PB4	I/O	Port B4	External Interrupt: EI3
10	PB5	I/O	Port B5	External Interrupt: EI3
11	PB6	I/O	Port B6	External Interrupt: EI3
12	PB7	I/O	Port B7	External Interrupt: EI3
13	PD0/AIN0	I/O	Port D0 or ADC Analog Input 0	
14	PD1/AIN1	I/O	Port D1 or ADC Analog Input 1	
15	PD2/AIN2	I/O	Port D2 or ADC Analog Input 2	
16	PD3/AIN3	I/O	Port D3 or ADC Analog Input 3	
17	PD4/AIN4	I/O	Port D4 or ADC Analog Input 4	
18	PD5/AIN5	I/O	Port D5 or ADC Analog Input 5	
19	PD6/AIN6	I/O	Port D6 or ADC Analog Input 6	
20	PD7/AIN7	I/O	Port D7 or ADC Analog Input 7	
21	V_{DDA}	S	Power Supply for analog peripheral (ADC)	
22	V_{SSA}	S	Ground for analog peripheral (ADC)	
23	V_{DDP_2}	S	Power Supply for Output Buffers (Ports B&E and PWM outputs)	
24	V_{SSP_2}	S	Ground for Output Buffers (Ports B&E and PWM outputs)	
25	PF0	I/O	Port F0	External Interrupt: EI1
26	PF1	I/O	Port F1	External Interrupt: EI1
27	PF2	I/O	Port F2	External Interrupt: EI1
28	NU		Non user pin. Must be left unconnected.	
29	PF4/OCMP1_A	I/O	Port F4 or Timer A Output Compare 1	
30	NU		Non user pin. Must be left unconnected.	
31	PF6/ICAP1_A	I/O	Port F6 or Timer A Input Capture 1	
32	PF7/EXTCLK_A	I/O	Port F7 or External Clock on Timer A	
33	V_{DDP_1}	S	Power Supply for Output Buffers (Ports C & F)	
34	V_{SSP_1}	S	Ground for Output Buffers (Ports C & F)	
35	PC0/OCMP2_B	I/O	Port C0 or Timer B Output Compare 2	
36	PC1/OCMP1_B	I/O	Port C1 or Timer B Output Compare 1	
37	PC2/ICAP2_B	I/O	Port C2 or Timer B Input Capture 2	
38	PC3/ICAP1_B	I/O	Port C3 or Timer B Input Capture 1	

Pin	Pin Name	Type	Description	Remarks
39	PC4/MISO	I/O	Port C4 or SPI Master In / Slave Out Data	
40	PC5/MOSI	I/O	Port C5 or SPI Master Out / Slave In Data	
41	PC6/SCK	I/O	Port C6 or SPI Serial Clock	
42	PC7/$\overline{SS}$	I/O	Port C7 or SPI Slave Select (active low)	
43	PA0	I/O	Port A0	External Interrupt: EI0
44	PA1	I/O	Port A1	External Interrupt: EI0
45	PA2	I/O	Port A2	External Interrupt: EI0
46	PA3	I/O	Port A3	External Interrupt: EI0
47	V_{DDP_0}	S	Power Supply for Output buffers (PA0 to PA3)	
48	V_{SSP_0}	S	Ground for Output buffers (Port A)	
49	PA4	I/O	Port A4	High Current
50	PA5	I/O	Port A5	High Current
51	PA6	I/O	Port A6	High Current
52	PA7	I/O	Port A7	High Current
53	TEST/V_{PP}[1)]	S	Test mode pin. In EPROM programming mode, this pin acts as the programming voltage input V_{PP}.	This pin should be tied low in user mode
54	$\overline{RESET}$	I/O	Bidirectional. Active low. Top priority non maskable interrupt.	
55	NC		Not Connected	
56	NC		Not Connected	
57	V_{SS}	S	Ground	
58	OSCOUT	I/O	Input/Output Oscillator pin.These pins connect a parallel resonant crystal, or an external source to the on-chip oscillator.	
59	OSCIN	I/O		
60	V_{DD}	S	Main power supply	
61	PE0/TDO	I/O	Port E0 or SCI Transmit Data Out	
62	PE1/RDI	I/O	Port E1 or SCI Receive Data In	
63	PE2/TXCAN	I	Port E2 or CAN Transmit Data Output	
64	PE3/RXCAN	I/O	Port E3 or CAN Receive Data Input	

Note 1: V_{PP} on EPROM/OTP only.

1.3 MEMORY MAP

Figure 3. Program Memory Map

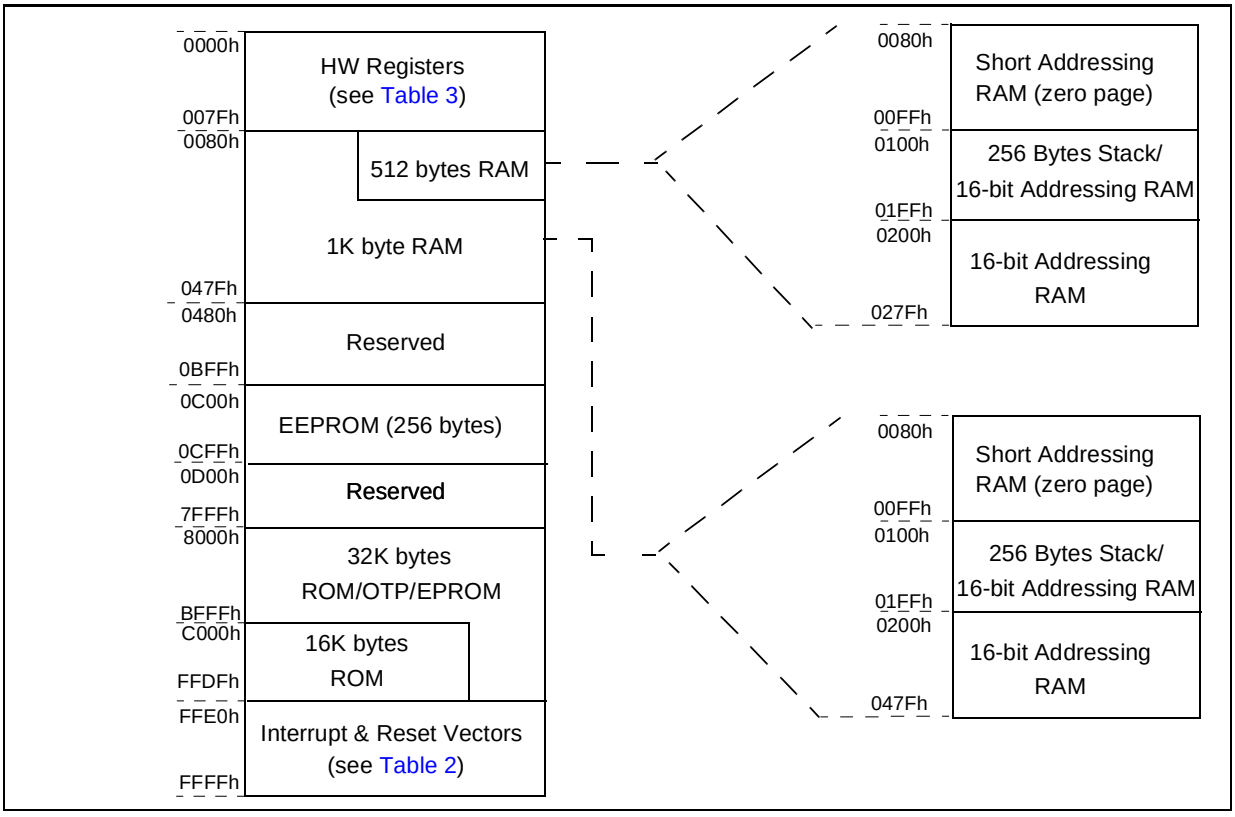


Table 2. Interrupt Vector Map

Vector Address	Description	Remarks
FFE0-FFE1h	Not Used	
FFE2-FFE3h	Not Used	
FFE4-FFE5h	EEPROM Programming Interrupt	Internal Interrupt
FFE6-FFE7h	SCI Interrupt Vector	Internal Interrupt
FFE8-FFE9h	TIMER B Interrupt Vector	Internal Interrupt
FFEA-FFEBh	TIMER A Interrupt Vector	Internal Interrupt
FFEC-FFEDh	SPI Interrupt Vector	Internal Interrupt
FFEE-FFEFh	CAN Interrupt Vector	Internal Interrupt
FFF0-FFF1h	External Interrupt Vector EI3 (PB4:PB7)	External Interrupt
FFF2-FFF3h	External Interrupt Vector EI2 (PB0:PB3)	External Interrupt
FFF4-FFF5h	External Interrupt Vector EI1 (PF0:PF2)	External Interrupt
FFF6-FFF7h	External Interrupt Vector EI0 (PA0:PA3)	External Interrupt
FFF8-FFF9h	Not Used	
FFFA-FFFBh	Not Used	
FFFC-FFFDh	TRAP (software) Interrupt Vector	CPU Interrupt
FFFE-FFFFh	RESET Vector	

Table 3. Hardware Register Memory Map

Address	Block	Register Label	Register name	Reset Status	Remarks
0000h 0001h 0002h 0003h	Port A	PADR PADDR PAOR	Data Register Data Direction Register Option Register Not Used	00h 00h 00h	R/W R/W R/W Absent
0004h 0005h 0006h 0007h	Port C	PCDR PCDDR	Data Register Data Direction Register Not Used Not Used	00h 00h	R/W R/W Absent Absent
0008h 0009h 000Ah 000Bh	Port B	PBDR PBDDR PBOR	Data Register Data Direction Register Option Register Not Used	00h 00h 00h	R/W R/W R/W Absent
000Ch 000Dh 000Eh 000Fh	Port E	PEDR PEDDR	Data Register Data Direction Register Not Used Not Used	00h 00h	R/W[1)] R/W[1)] Absent Absent
0010h 0011h 0012h 0013h	Port D	PDDR PDDDR	Data Register Data Direction Register Not Used Not Used	00h 00h	R/W R/W Absent Absent
0014h 0015h 0016h 0017h	Port F	PFDR PFDDR PFOR	Data Register Data Direction Register Option Register Not Used	00h 00h 00h	R/W R/W R/W Absent
0018h to 001Fh	Reserved Area (8 Bytes)				
0020h		MISCR	Miscellaneous Register	00h	
0021h 0022h 0023h	SPI	SPIDR SPICR SPISR	SPI Data I/O Register SPI Control Register SPI Status Register	xxh 0xh 00h	R/W R/W Read Only
0024h 0025h 0026h 0027h 0028h 0029h	PWMB	PWM0 BRM10 PWM1 PWM2 BRM32 PWM3	Pulse Binary Weight Register 0 BRM Register 10 Pulse Binary Weight Register 1 Pulse Binary Weight Register 2 BRM Register 32 Pulse Binary Weight Register 3	80h 00h 80h 80h 00h 80h	R/W R/W R/W R/W R/W R/W
002Ah 002Bh	WDG	WDGCR	Watchdog Control Register Not Used	7Fh	R/W
002Ch to 0030h	Reserved Area (5 Bytes)				
0031h 0032h 0033h 0034h-0035h 0036h-0037h	Timer A	TACR2 TACR1 TASR TAIC1HR TAIC1LR TAOC1HR TAOC1LR	Control Register2 Control Register1 Status Register Input Capture1 High Register Input Capture1 Low Register Output Compare1 High Register Output Compare1 Low Register	00h 00h xxh xxh xxh 80h 00h	R/W R/W Read Only Read Only Read Only R/W R/W

Address	Block	Register Label	Register name	Reset Status	Remarks
0038h-0039h	Timer A	TACHR	Counter High Register	FFh	Read Only
		TACLR	Counter Low Register	FCh	Read Only
003Ah-003Bh		TAACHR	Alternate Counter High Register	FFh	Read Only
		TAACLR	Alternate Counter Low Register	FCh	Read Only
003Ch-003Dh		TAIC2HR	Input Capture2 High Register	xxh	Read Only[2]
		TAIC2LR	Input Capture2 Low Register	xxh	Read Only[2]
003Eh-003Fh		TAOC2HR	Output Compare2 High Register	80h	R/W[2]
		TAOC2LR	Output Compare2 Low Register	00h	R/W[2]
0040h	Reserved Area				
0041h	Timer B	TBCR2	Control Register2	00h	R/W
0042h		TBCR1	Control Register1	00h	R/W
0043h		TBSR	Status Register	xxh	Read Only
0044h-0045h		TBIC1HR	Input Capture1 High Register	xxh	Read Only
		TBIC1LR	Input Capture1 Low Register	xxh	Read Only
0046h-0047h		TBOC1HR	Output Compare1 High Register	80h	R/W
		TBOC1LR	Output Compare1 Low Register	00h	R/W
0048h-0049h		TBCHR	Counter High Register	FFh	Read Only
		TBCLR	Counter Low Register	FCh	Read Only
004Ah-004Bh		TBACHR	Alternate Counter High Register	FFh	Read Only
		TBACLR	Alternate Counter Low Register	FCh	Read Only
004Ch-004Dh		TBIC2HR	Input Capture2 High Register	xxh	Read Only
		TBIC2LR	Input Capture2 Low Register	xxh	Read Only
004Eh-004Fh		TBOC2HR	Output Compare2 High Register	80h	R/W
		TBOC2LR	Output Compare2 Low Register	00h	R/W
0050h	SCI	SCISR	SCI Status Register	C0h	Read Only
0051h		SCIDR	SCI Data Register	xxh	R/W
0052h		SCIBRR	SCI Baud Rate Register	00x----xb	R/W
0053h		SCICR1	SCI Control Register 1	xxh	R/W
0054h		SCICR2	SCI Control Register 2	00h	R/W
0055h		SCIERPR	SCI Extended Receive Prescaler Register	00h	R/W
0056h			Reserved	---	Reserved
0057h		SCIETPR	SCI Extended Transmit Prescaler Register	00h	R/W
0058h to 0059h	Reserved Area (2 Bytes)				
005Ah	CAN	CANISR	CAN Interrupt Status Register	00h	R/W
005Bh		CANICR	CAN Interrupt Control Register	00h	R/W
005Ch		CANCSR	CAN Control/Status Register	00h	R/W
005Dh		CANBRPR	CAN Baud Rate Prescaler Register	00h	R/W
005Eh		CANBTR	CAN Bit Timing Register	23h	R/W
005Fh		CANPSR	CAN Page Selection	00h	R/W
0060h to 006Fh			CAN First address to last address of PAGE X	--	
0070h to 007Fh	Reserved Area (16 Bytes)				

Notes:

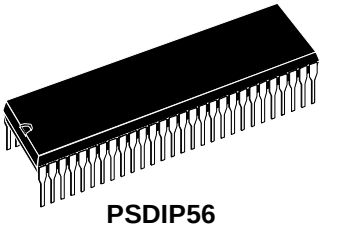
1. The bits corresponding to unavailable pins are forced to zero by hardware.
2. External pin not available.

ST72671

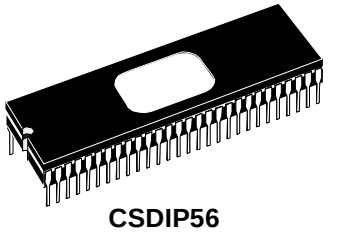
8-BIT USB MCUs WITH 16K TO 32K ROM/OTP/EPROM, 512 BYTES TO 1K RAM, ADC, DAC (PWM), TIMER, I^2C AND SCI

PRODUCT PREVIEW

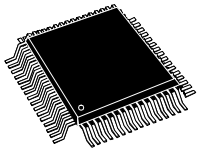
- User Program Memory ROM/OTP/EPROM: 16K to 32K bytes
- Data RAM: 512 bytes to 1K byte (256 bytes stack)
- Master Reset and Power on/off reset
- Run, Wait, Slow, Halt and RAM Retention modes
- USB (Universal Serial Bus) with 2 endpoints including:
  - Integrated 3.3V voltage regulator
  - Integrated Transceiver
  - Suspend and Resume operations
- 32 I/O lines
  - 5 programmable interrupt inputs
  - 8 high sink outputs
  - 8 analog alternate inputs
  - 18 alternate functions
  - EMI filtering
- Programmable Watchdog (WDG)
- 16-bit Timer, featuring:
  - 2 Input Captures
  - 2 Output Compares (with 1 output pin)
  - PWM and Pulse Generator modes
- 8-bit Analog to Digital Converter with 8 channels on port B
- Four 10-bit and one 12-bit Digital to Analog Converter Channels with PWM output
- Fast I^2C Multi Master Interface
- Serial Communications Interface (SCI)
- 63 basic instructions
- 17 main address modes
- 8x8 unsigned multiply instruction
- True bit manipulation
- Complete Development Support on PC/DOS-WINDOWS™ Real-Time Emulator
- Full Software Package on DOS/WINDOWS™ (C-Compiler, Cross-Assembler, Debugger)



PSDIP56



CSDIP56



TQFP64

Device Summary

Features	ST72671N4	ST72671N6
Program memory -bytes	16K	32K
RAM (stack) - bytes	512 (256)	1K (256)
USB	2 endpoints	
10-Bit D/A Converter	4 channels	
12-Bit D/A Converter	1 channel	
A/D Converter	8 channels	
16-Bit Timer	1	
I^2C Bus	1 multimaster	
I/Os	34	
Operating Supply	4.0 to 5.5 V	
CPU Frequency	8 MHz max (24 MHz quartz)	
Temperature Range	0°C to + 70°C	
Package	QFP64 - SDIP56	

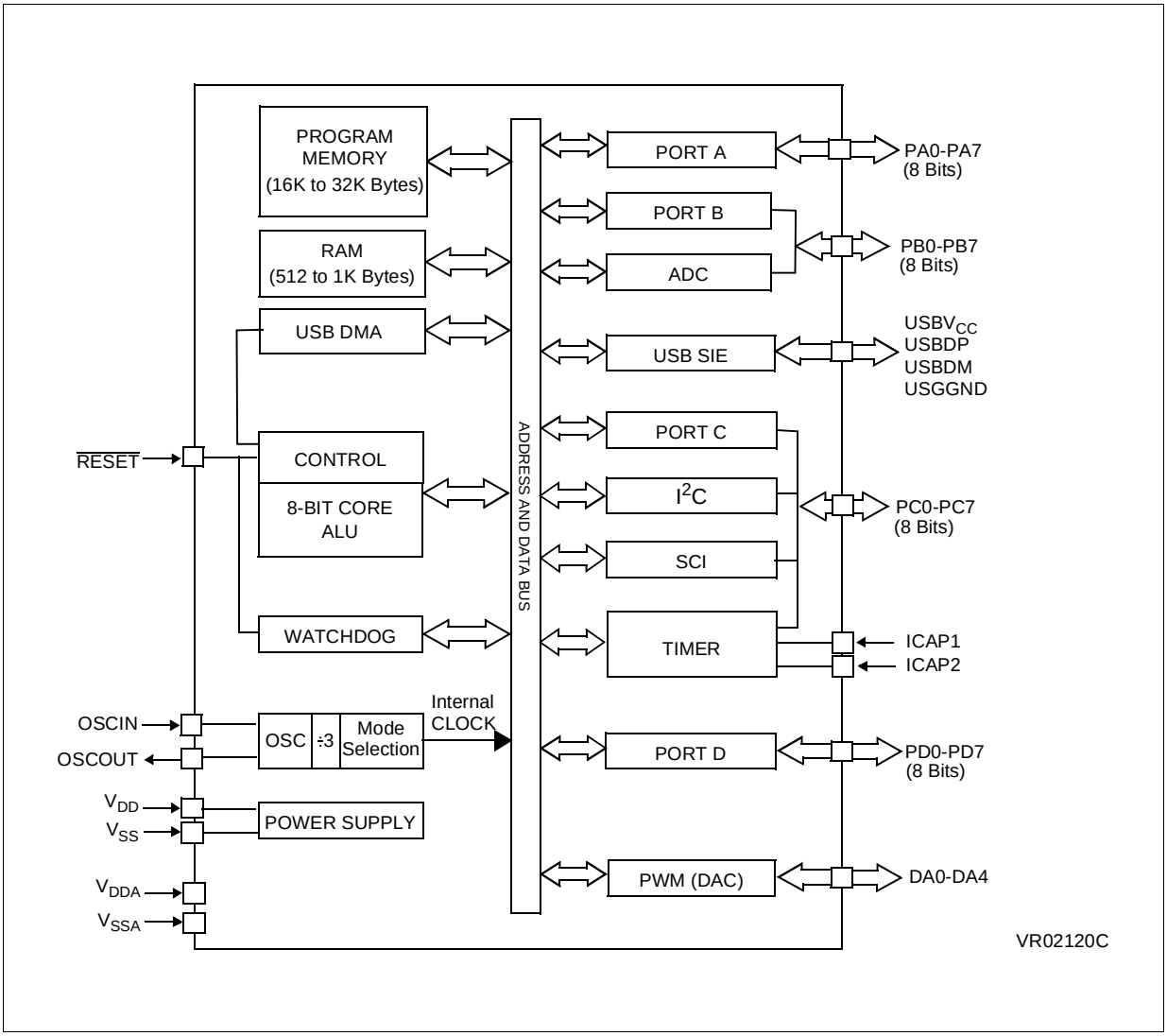
1 GENERAL DESCRIPTION

1.1 INTRODUCTION

The ST72671 HCMOS microcontroller unit is a member of the ST7 family with an integrated USB interface.
It is based around an industry standard 8-bit core and offers an enhanced instruction set. The processor runs with an external clock up to 24 MHz with a 5V supply. Due to the fully static design of this device, operation down to DC is possible. Under software control the ST72671 can be placed in WAIT, SLOW or HALT mode thus reducing power consumption. The enhanced instruction set and addressing modes afford real programming potential.

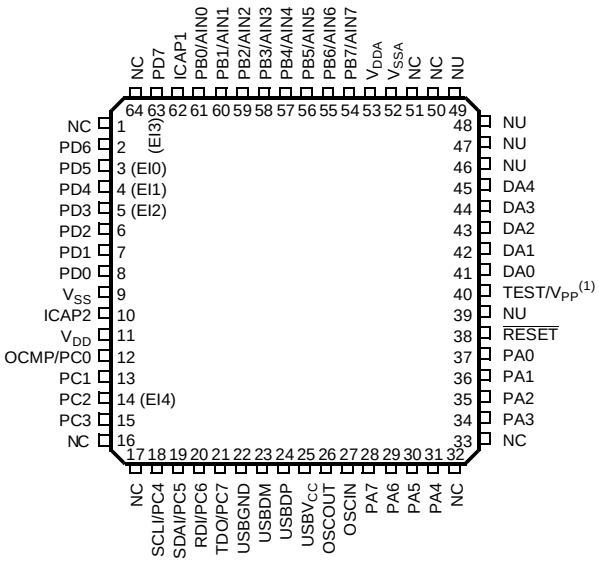
In addition to standard 8-bit data management the ST7 features true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes on the whole memory.
The device includes an on-chip oscillator, CPU, 16K to 32K ROM/OTP/EPROM, 512 to 1K RAM, USB, 32 I/O lines, a Timer with 2 Input Captures and 2 Output Compares, an 8-channel A/D Converter, an I^2C multimaster, an SCI Serial Communications Interface, a Watchdog Reset, four 10-bit and one 12-bit D/A Converter channels with PWM output.

Figure 1. ST72671 Block Diagram



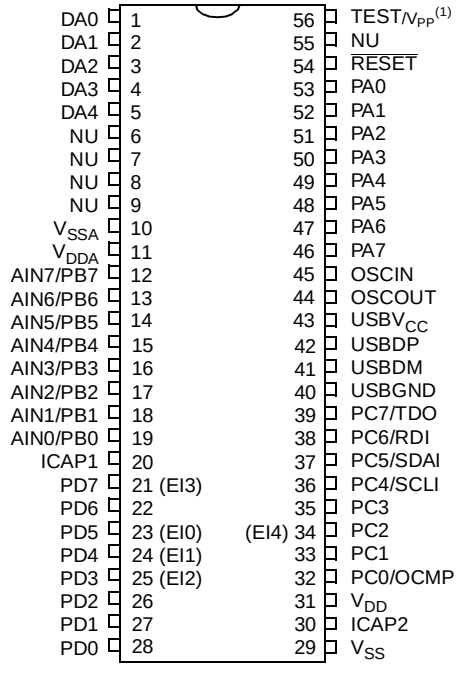
1.2 PIN DESCRIPTION

Figure 2. 64-Pin QFP Package Pinout



(1) V_{PP} on EPROM/OTP only

Figure 3. 56-Pin SDIP Package Pinout



(1) V_{PP} on EPROM/OTP only

Note: Several pins of the I/O ports assume software programmable alternate functions as shown in the pin description.

PIN DESCRIPTION (Cont'd)

Table 1. ST72671N Pin Description

Pin n° QFP64	Pin n° SDIP56	Pin Name	Type	Description	Remarks
1		NC		Not Connected	
2	22	PD6	I/O	Port D6	
3	23	PD5	I/O	Port D5 or Interrupt falling edge detector input	External Interrupt: EI0
4	24	PD4	I/O	Port D4 or Interrupt falling edge detector input	External Interrupt: EI1
5	25	PD3	I/O	Port D3 or Interrupt falling edge detector input	External Interrupt: EI2
6	26	PD2	I/O	Port D2	
7	27	PD1	I/O	Port D1	
8	28	PD0	I/O	Port D0	
9	29	V_{SS}	S	Ground	
10	30	ICAP2		Timer Input Capture 2 with 256 prescaler	Not for general purpose I/O
11	31	V_{DD}	S	Main power supply	
12	32	PC0/OCMP	I/O	Port C0 or Timer Output Compare	
13	33	PC1	I/O	Port C1	
14	34	PC2	I/O	Port C2 or Interrupt falling edge detector input	External Interrupt: EI4
15	35	PC3	I/O	Port C3	
16		NC		Not Connected	
17		NC		Not Connected	
18	36	PC4/SCLI	I/O	Port C4 or I^2C Serial Clock	
19	37	PC5/SDAI	I/O	Port C5 or I^2C Serial Data	
20	38	PC6/RDI	I/O	Port C6 or SCI Receive Data Input	
21	39	PC7/TDO	I/O	Port C7 or SCI Transmit Data Output	
22	40	USBGND	S	USB ground	
23	41	USBDM	I/O	USB bidirectional data	
24	42	USBDP	I/O	USB bidirectional data	
25	43	$USBV_{CC}$	S	USB power supply (output, 3.3V+/- 10%). This pin requires an external 4.7µF decoupling capacitor to ground, and can be only connected to the external USB pull-up resistor.	
26	44	OSCOUT	O	Input/Output Oscillator pin. These pins connect a parallel-resonant crystal, or an external source to the on-chip oscillator.	
27	45	OSCIN	I		
28	46	PA7	I/O	Port A7	High Sink
29	47	PA6	I/O	Port A6	High Sink
30	48	PA5	I/O	Port A5	High Sink
31	49	PA4	I/O	Port A4	High Sink
32		NC		Not Connected	
33		NC		Not Connected	
34	50	PA3	I/O	Port A3	High Sink
35	51	PA2	I/O	Port A2	High Sink

Pin n° QFP64	Pin n° SDIP56	Pin Name	Type	Description	Remarks
36	52	PA1	I/O	Port A1	High Sink
37	53	PA0	I/O	Port A0	High Sink
38	54	$\overline{\text{RESET}}$	I/O	Bidirectional. Active low. Top priority non maskable interrupt.	Can be used to reset external peripherals.
39	55	NU		Non User Pin. Must be connected to V_{CC}	
40	56	TEST/V_{PP}	S	Test mode pin. In the EPROM programming mode, this pin acts as the programming voltage input V_{PP}.	This pin should be tied low in user mode
41	1	DA0	O	12-bit D/A (PWM output)	For analog controls, after external filtering
42	2	DA1	O	10-bit D/A (PWM output)	
43	3	DA2	O	10-bit D/A (PWM output)	
44	4	DA3	O	10-bit D/A (PWM output)	
45	5	DA4	O	10-bit D/A (PWM output)	
46	6	NU		Non User pin. Must be left unconnected	
47	7	NU		Non User pin. Must be left unconnected	
48	8	NU		Non User pin. Must be left unconnected	
49	9	NU		Non User pin. Must be left unconnected	
50		NC		Not Connected	
51		NC		Not Connected	
52	10	V_{SSA}	S	Ground for analog peripheral (ADC)	Must be connected externally to V_{SS}
53	11	V_{DDA}	S	Power Supply for analog peripheral (ADC)	Must be connected externally to V_{DD}
54	12	PB7/AIN7	I/O	Port B7 or ADC analog input 7	
55	13	PB6/AIN6	I/O	Port B6 or ADC analog input 6	
56	14	PB5/AIN5	I/O	Port B5 or ADC analog input 5	
57	15	PB4/AIN4	I/O	Port B4 or ADC analog input 4	
58	16	PB3/AIN3	I/O	Port B3 or ADC analog input 3	
59	17	PB2/AIN2	I/O	Port B2 or ADC analog input 2	
60	18	PB1/AIN1	I/O	Port B1 or ADC analog input 1	
61	19	PB0/AIN0	I/O	Port B0 or ADC analog input 0	
62	20	ICAP1		Timer Input Capture 1	Not for general purpose I/O
63	21	PD7	I/O	Port D7 or Interrupt rising edge detector input	External Interrupt: EI3
64		NC		Not Connected	

Note: S=Supply

1.3 MEMORY MAP

Figure 4. Program Memory Map

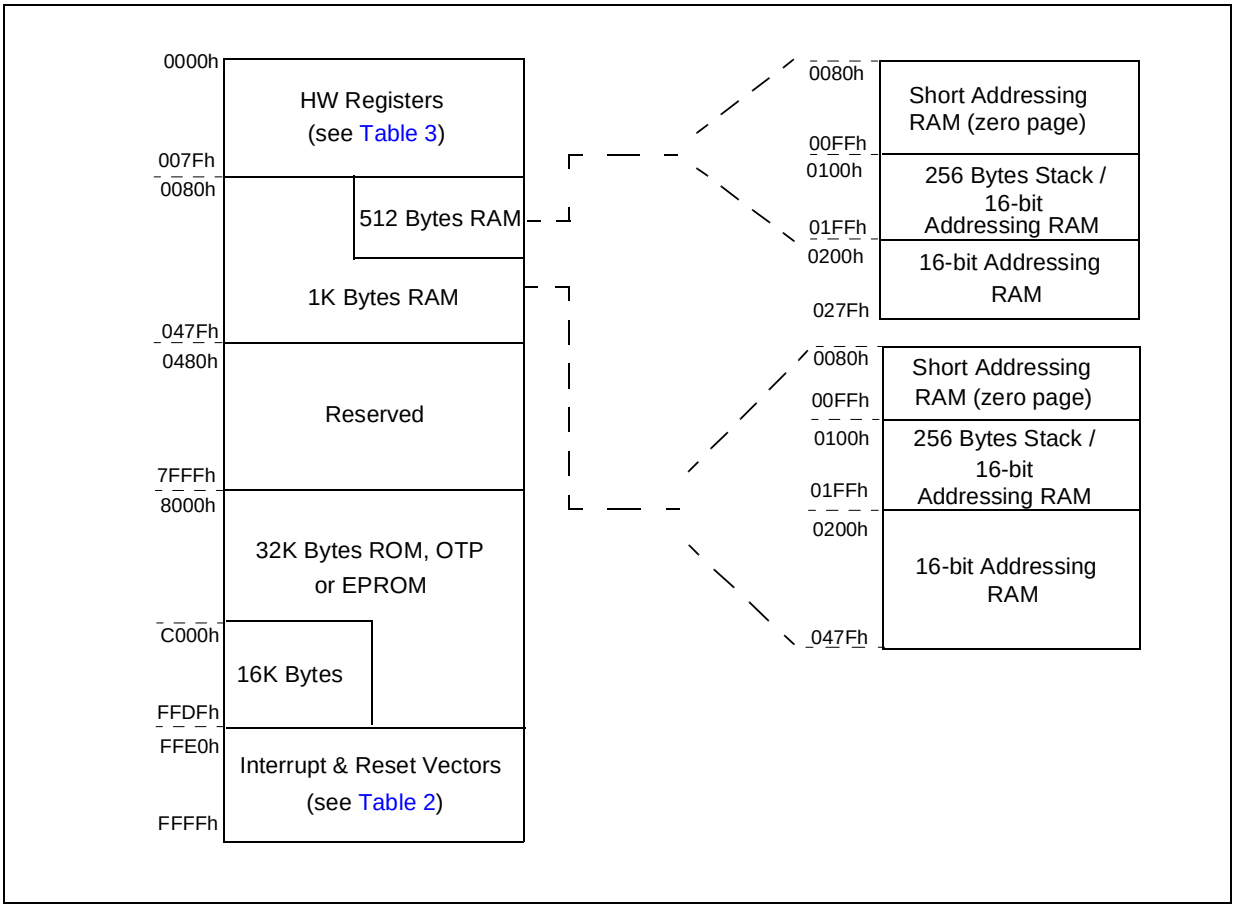


Table 2. Interrupt Vector Map

Vector Address	Description	Remarks
FFE0-FFE1h	USB Interrupt Vector	Internal Interrupt
FFE2-FFE3h	SCI Interrupt Vector	"
FFE4-FFE5h	I^2C Interrupt Vector	"
FFE6-FFE7h	Timer Overflow Interrupt Vector	"
FFE8-FFE9h	Timer Output Compare Interrupt Vector	"
FFEA-FFEBh	Timer Input Capture Interrupt Vector	"
FFEC-FFEDh	Reserved	
FFEE-FFEFh	EI4 Interrupt Vector	External Interrupt
FFF0-FFF1h	EI0 Interrupt Vector	"
FFF2-FFF3h	EI1 Interrupt Vector	"
FFF4-FFF5h	EI2 Interrupt Vector	"
FFF6-FFF7h	EI3 Interrupt Vector	"
FFF8-FFF9h	Reserved	
FFFA-FFFBh	USB End Suspend Interrupt Vector	Internal Interrupt
FFFC-FFFDh	TRAP Interrupt Vector	Software interrupt
FFFE-FFFFh	RESET Vector	CPU Interrupt

MEMORY MAP (Cont'd)

Table 3. Hardware Register Memory Map

Address	Block	Register Label	Register Name	Reset Status	Remarks
0000h 0001h	Port A	PADR PADDR	Port A Data Register Port A Data Direction Register	00h 00h	R/W R/W
0002h 0003h	Port C	PCDR PCDDR	Port C Data Register Port C Data Direction Register	00h 00h	R/W R/W
0004h 0005h	Port D	PDDR PDDDR	Port D Data Register Port D Data Direction Register	00h 00h	R/W R/W
0006h 0007h 0008h	Port B	PBDR PBDDR PBICFGR	Port B Data Register Port B Data Direction Register Port B Input Pull-Up Configuration Register	00h 00h 00h	R/W R/W R/W
0009h		MISCR	Miscellaneous Register	00h	R/W
000Ah 000Bh	ADC	ADCDR ADCCSR	ADC Data Register ADC Control Status register	00h 00h	Read only R/W
000Ch	WDG	WDGCR	Watchdog Control Register	7Fh	R/W
000Dh to 000Fh	Reserved Area (3 bytes)				
00010h	ITR	ITRFRE	Interrupt Register	00h	R/W
0011h 0012h 0013h 0014h 0015h 0016h 0017h 0018h 0019h 001Ah 001Bh 001Ch 001Dh 001Eh 001Fh	TIM	TIMCR2 TIMCR1 TIMSR TIMIC1HR TIMIC1LR TIMOC1HR TIMOC1LR TIMCHR TIMCLR TIMACHR TIMACLR TIMIC2HR TIMIC2LR TIMOC2HR TIMOC2LR	Timer Control Register 2 Timer Control Register 1 Timer Status Register Timer Input Capture 1 High Register Timer Input Capture 1 Low Register Timer Output Compare 1 High Register Timer Output Compare 1 Low Register Timer Counter High Register Timer Counter Low Register Timer Alternate Counter High Register Timer Alternate Counter Low Register Timer Input Capture 2 High Register Timer Input Capture 2 Low Register Timer Output Compare 2 High Register Timer Output Compare 2 Low Register	00h 00h 00h xxh xxh 80h 00h FFh FCh FFh FCh xxh xxh 80h 00h	R/W R/W Read only Read only Read only R/W R/W Read only Read only Read only Read only Read only Read only R/W R/W
0020h 0021h	Reserved Area (2 bytes)				
0022h 0023h	DAC	PWM0 BRM0	12-BIT PWM Register 12-BIT BRM Register	80h C0h	R/W R/W
0024h 0025h 0026h 0027h 0028h 0029h		PWM1 BRM21 PWM2 PWM3 BRM43 PWM4	10-BIT PWM / BRM Registers	80h 00h 80h 80h 00h 80h	R/W R/W R/W R/W R/W R/W
002Ah to 002Fh	Reserved Area (6 bytes)				

Address	Block	Register Label	Register Name	Reset Status	Remarks
0030h	SCI	SCISR	SCI Status Register	C0h	Read only
0031h		SCIDR	SCI Data Register	xxh	R/W
0032h		SCIBRR	SCI Baud Rate Register	00xx xxxx	R/W
0033h		SCICR1	SCI Control Register 1	xxh	R/W
0034h		SCICR2	SCI Control Register 2	00h	R/W
0035h	USB	USBPIDR	USB PID Register	xx00 0000	Read only
0036h		USBDMAR	USB DMA address Register	xxh	R/W
0037h		USBIDR	USB Interrupt/DMA Register	x0h	R/W
0038h		USBISTR	USB Interrupt Status Register	00h	R/W
0039h		USBIMR	USB Interrupt Mask Register	00h	R/W
003Ah		USBCTLR	USB Control Register	06h	R/W
003Bh		USBDADDR	USB Device Address Register	00h	R/W
003Ch		USBEP0RA	USB Endpoint 0 Register A	0xh	R/W
003Dh		USBEP0RB	USB Endpoint 0 Register B	80h	R/W
003Eh		USBEP1RA	USB Endpoint 1 Register A	0xh	R/W
003Fh		USBEP1RB	USB Endpoint 1 Register B	0xh	R/W
0040h to 0042h	Reserved Area (3 bytes)				
0043h	TIM	CONFIG	ICAP Configuration **Warning:** Write 0Ch in this register to use the ICAP1 and ICAP2 functions.	08h	R/W
0044h to 0058h	Reserved Area (21 bytes)				
0059h	I^2C	I2CDR	I^2C Data Register	00h	R/W
005Ah			Reserved		
005Bh		I2COAR	I^2C (7 Bits) Slave Address Register	00h	R/W
005Ch		I2CCCR	I^2C Clock Control Register	00h	R/W
005Dh		I2CSR2	I^2C Status Register 2	00h	Read only
005Eh		I2CSR1	I^2C Status Register 1	00h	Read only
005Fh		I2CCR	I^2C Control Register	00h	R/W
0060h to 007Fh	Reserved Area (32 bytes)				